Advanced Techniques for PCIe 3.0 Receiver Testing

Michael Fleischer-Reumann

BERTs Portfolio Planner

Agilent Technologies

Disclaimer

Presentation Disclaimer: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of the PCI-SIG®.

Agenda

- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

From PCIe 2.x to PCIe 3.0 - Goals and Consequences

Goals

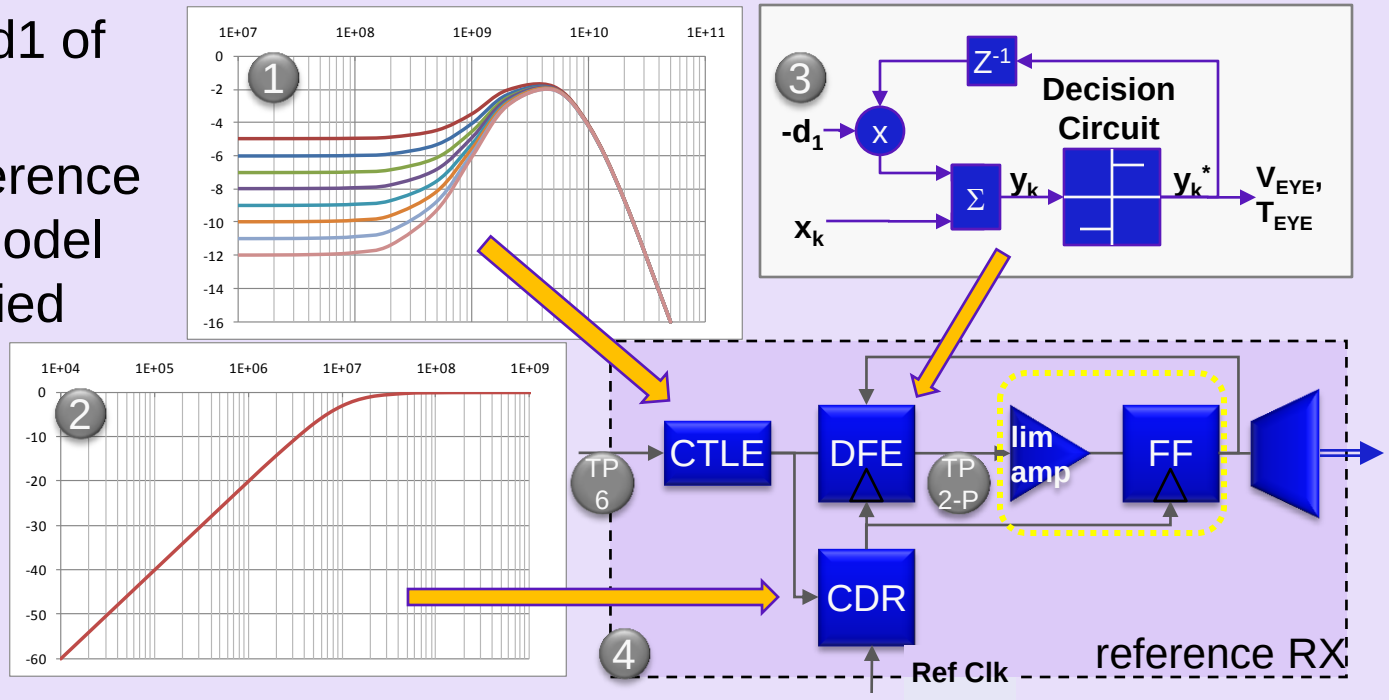
- Effective data rate shall be doubled
- Existing infrastructure of PCs and servers shall be reusable; in PCIe terminology this means:
  - ✓ PCIe 2.x compliant channels shall also be compliant with PCIe 3.0

Consequences

- Transmitting data at higher rate over the same channels means more loss causing closed eyes at the end of channel / receiver (RX) input
- Method needs to be found opening the signal eye in order to
  - ✓ asses channel compliance
  - ✓ achieve functionality
- Circuits and methods compensating channel loss have to be implemented in active components, Transmitter (TX) and Receiver (RX)
  - ✓ enhancing TX de-emphasis range and adding pre-shoot not sufficient
  - ⇨ **extensive RX equalization is necessary to achieve functionality**
  - ✓ open source simulation tool (seasim) provides turnkey capability for channel assessment, where the user provides the channel characteristics at the receiver's die pad as step responses, and the tool calculates a statistical eye showing pass/fail.

Reference Receiver with Equalization

1. CTLE with seven “DC-attenuation“ settings peaking at 4 GHz
2. Reference CDR specified by OJTF with no peaking and 10MHz BW
3. One tap DFE with a limit for d1 of +/- 30mV
4. Π-type reference package model also specified

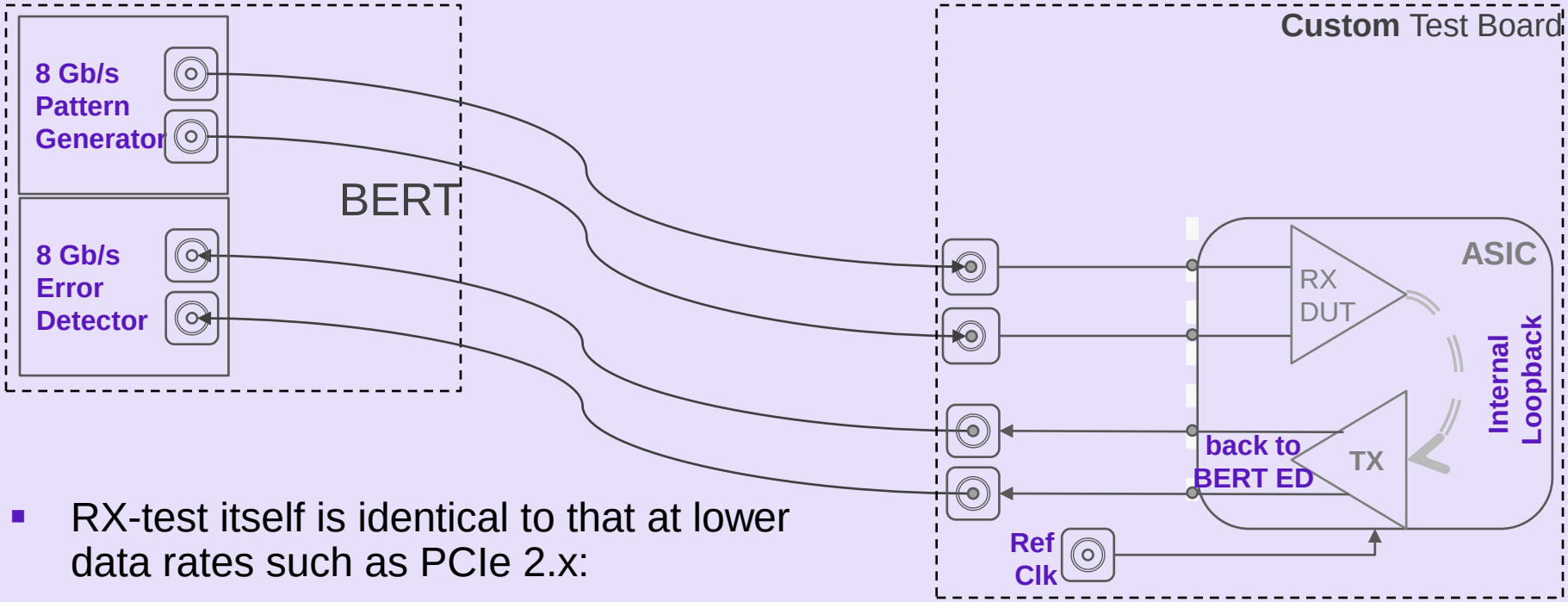


Eye opening is specified for basic RX inside orange dotted box

Agenda

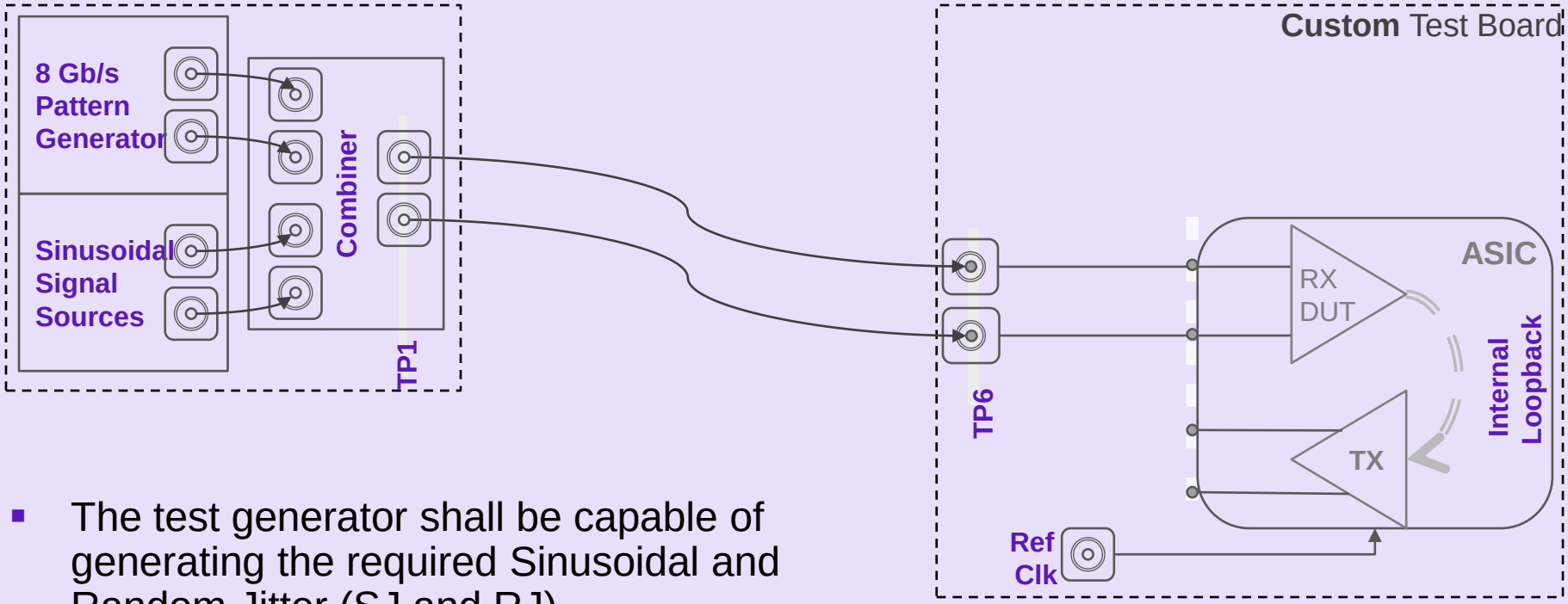
- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

RX Test for PCIe 3.0 Generic Test Set-up



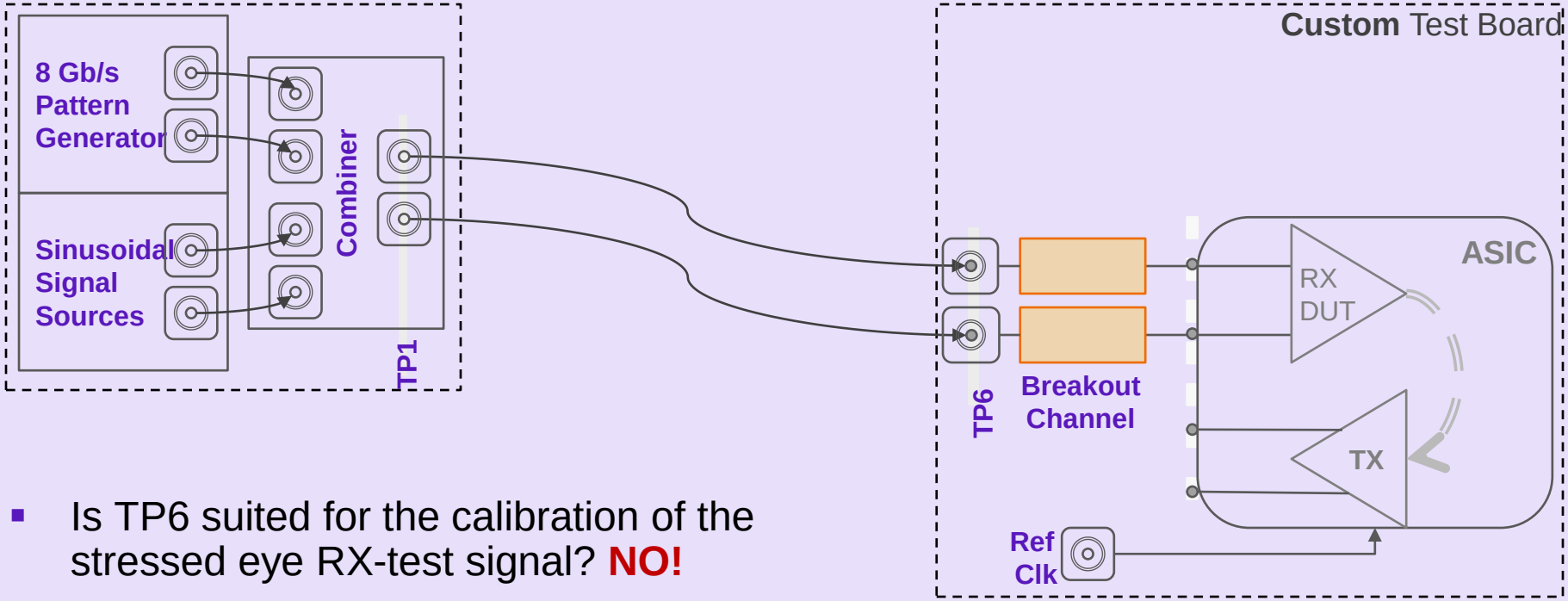
- RX-test itself is identical to that at lower data rates such as PCIe 2.x:
  - ✓ RX input is stimulated from a BERT PG with a “stressed eye“ signal containing well defined impairments
  - ✓ RX-output is looped back through the device’s TX such that the RX’s “correct” detection can be observed with a Bit Error Ratio Tester (BERT)
- Construction / calibration of RX stress test signal is completely different utilizing methods and tools originally created for channel compliance verification

RX Test-set-up acc. to PCIe 3.0 Base Spec.



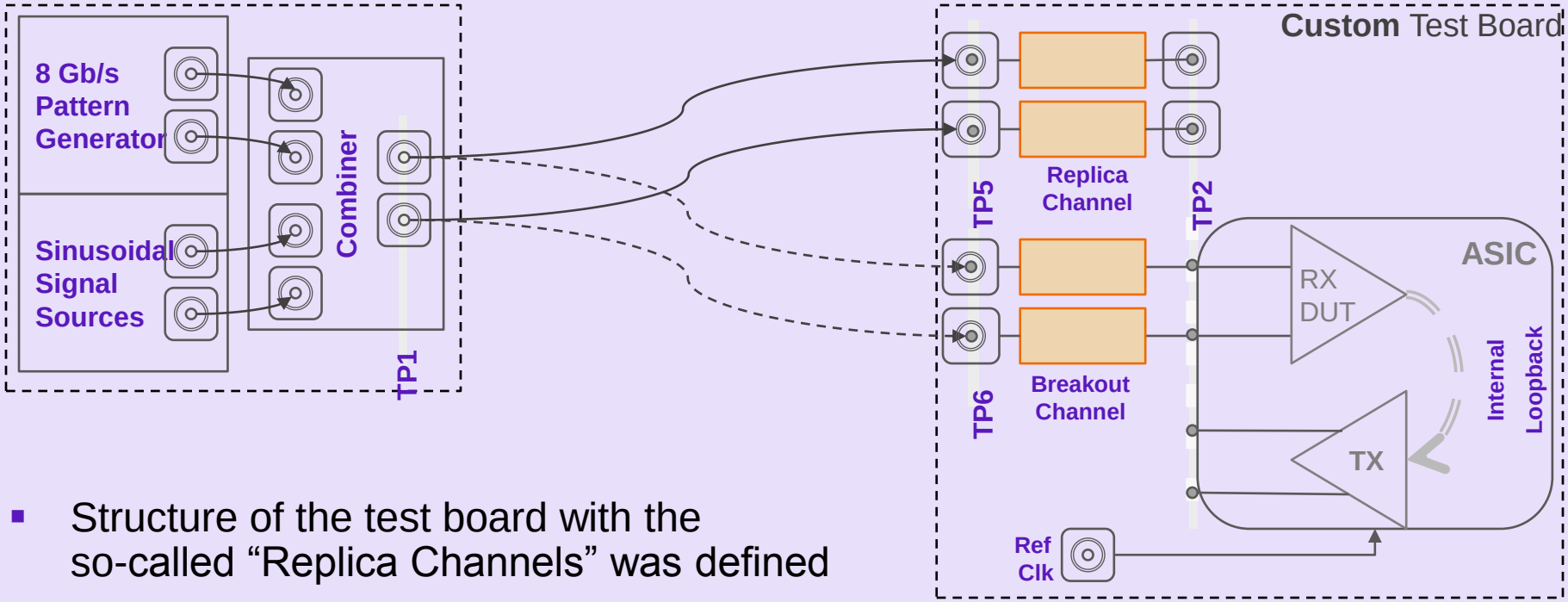
- The test generator shall be capable of generating the required Sinusoidal and Random Jitter (SJ and RJ)
- It is complemented with signal sources for the simultaneous generation of Common- and Differential Mode Sinusoidal Interference (CM- and DM-SI) modeling the “noise” of the real application
- They are superimposed to the test pattern through a passive combiner; output at TP1
- Is TP6 suited for the calibration of the stressed eye RX-test signal?

RX Test-set-up acc. to PCIe 3.0 Base Spec.



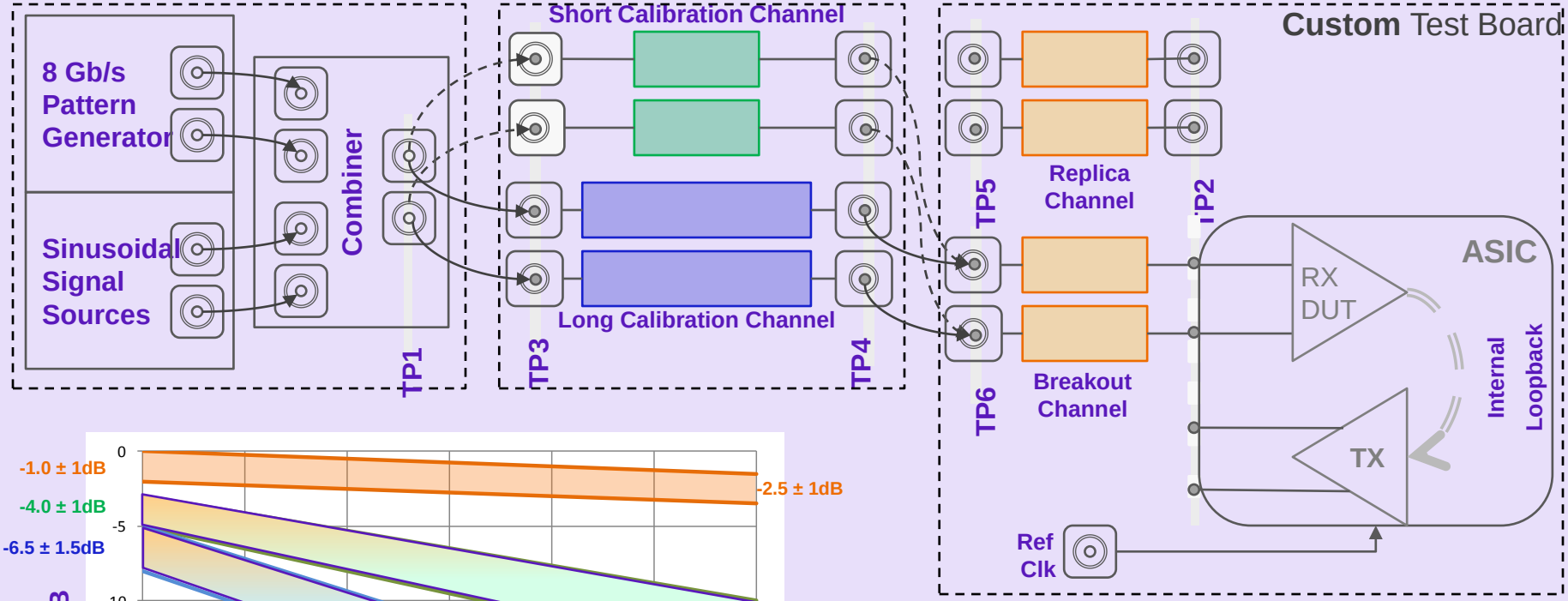
- Is TP6 suited for the calibration of the stressed eye RX-test signal? **NO!**
- The PC board traces enabling connection of the DUT with test equipment (the so-called breakout channels) are not negligible in terms of signal degradation (DDJ) / (ISI)
- Calibration must include the breakout channels
- Connecting or probing for calibration of the stress signal directly at the ASIC pins / balls is not practical!

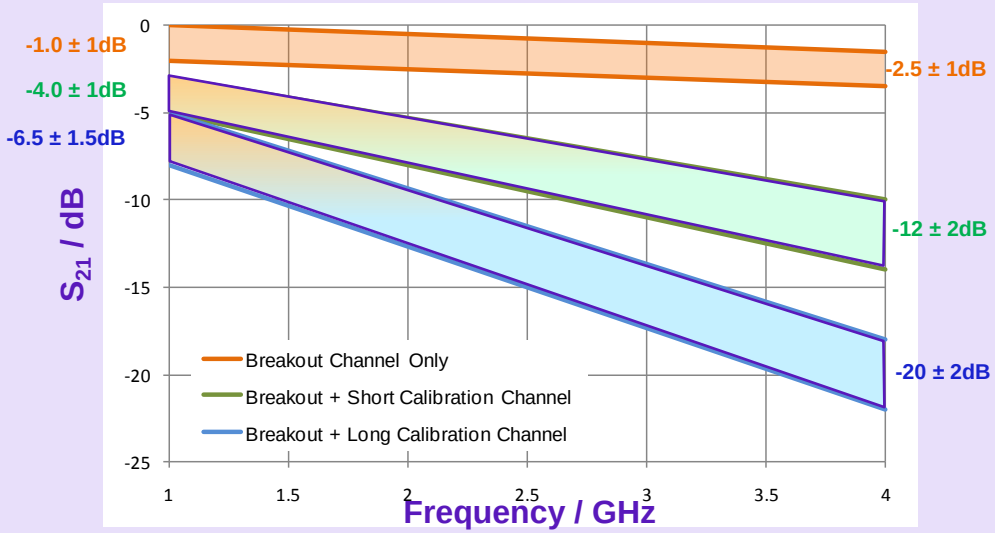
RX Test-set-up acc. to PCIe 3.0 Base Spec.



- Structure of the test board with the so-called “Replica Channels” was defined
- At the output of those there is the important test point TP2
- TP2 is equivalent to the ASIC-input pins / balls as the replica channels duplicate the break-out channels
- TP2 is the “closest point” to the RX inputs that can be measured of the RX test signals

RX Test-set-up acc. to PCIe 3.0 Base Spec.





Emulation of different target applications is achieved with different channel lengths: Three test cases have been defined :

- Break-out channel only (2.5dB @ 4GHz)
- Break-out + short cal chan. (9.5dB @ 4GHz)
- Break-out + long cal chan. (17.5dB @ 4GHz)

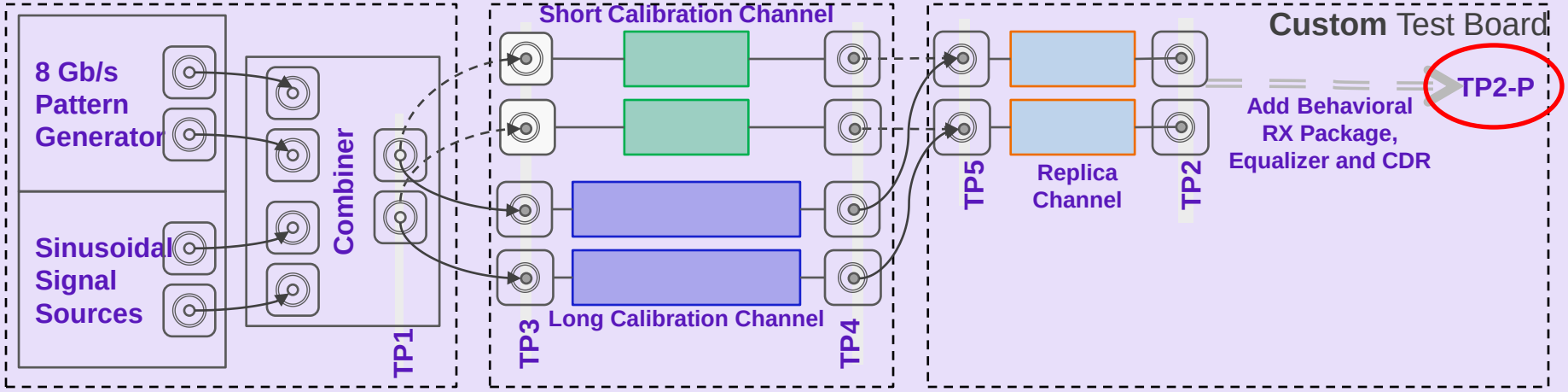
RX Test Specifications for Stressed *Jitter* Eye

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800 (nominal)	mV_{PP}	Measured at TP1,
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye height at TP2P	25 (min) 35 (max)	mV_{PP}	At BER=10^{-12}
$T_{RX-SV-8G}$	Eye width at TP2P	0.30	UI	At BER=10^{-12}
$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 – 1.0	UI_{PP}	Measured at TP1.
$T_{RX-SV--RJ-8G}$	Random Jitter	3.0	ps_{RMS}	RJ spectrally flat before filtering. Measured at TP1. Adjusted to set eye width

RX Test Specifications for Stressed *Voltage* Eye

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator launch voltage	800	mV_{PP}	Measured at TP1 Figure 4-65. VRX-LAUNCH-8G may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mV_{PP}.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mV_{PP}	Eye height @ BER=10^{-12}
$T_{RX-SV-8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER=10^{-12}.
$V_{RX-SV-DIFF-8G}$	Differential mode interference	14 or greater	mV_{PP}	Adjusted to set EH. Frequency = 2.10 GHz..
$V_{RX-SV-CM-8G}$	Rx AC Common mode voltage at 120MHz at TP2P	150 (EH < 100 mV_{PP}) 250 (EH ≥ 100 mV_{PP})	mV_{PP}	Defined for a single tone at 120 MHz.
$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI_{PP}	Fixed at 100 MHz.
$T_{RX-SV--RJ-8G}$	Random Jitter	2.0	ps_{RMS}	Rj spectrally flat before filtering.

Calibration Method of Stressed Eye for RX Test



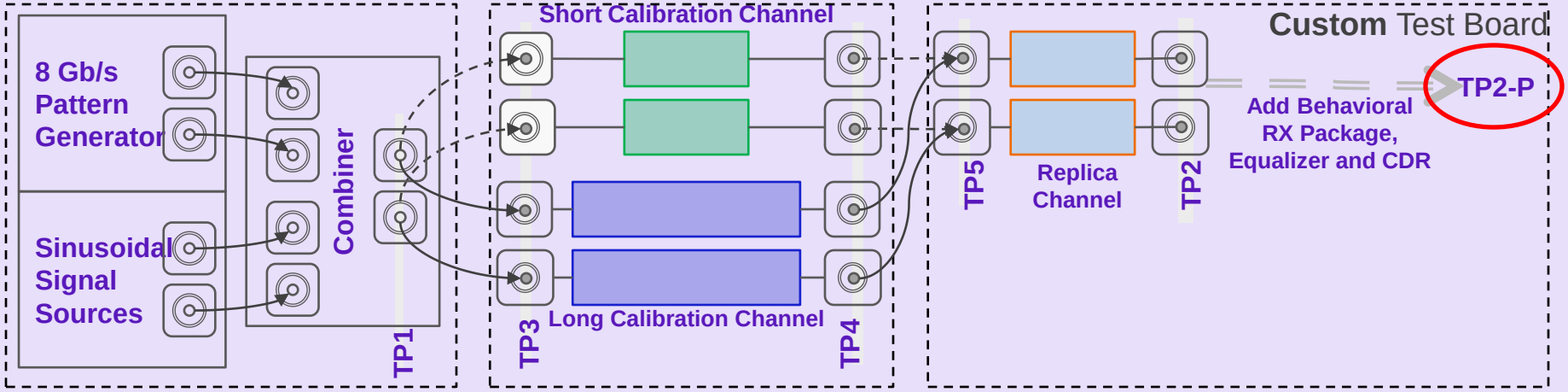
- When using long calibration channel signal eye at TP2 is completely closed
- Specifying stressed eye or jitter components at TP2 is therefore impractical

⇨ Specification of minimal tolerable eye opening refers to input of “basic receiver” inside the ASIC behind the reference RX’s equalization (CTLE and DFE) and “jitter-filtering” with OJTF of RX-CDR
(post processed signal of TP2 resulting in the signal at virtual test point TP2-P)

⇨ Calibration by measurement *only* is not possible

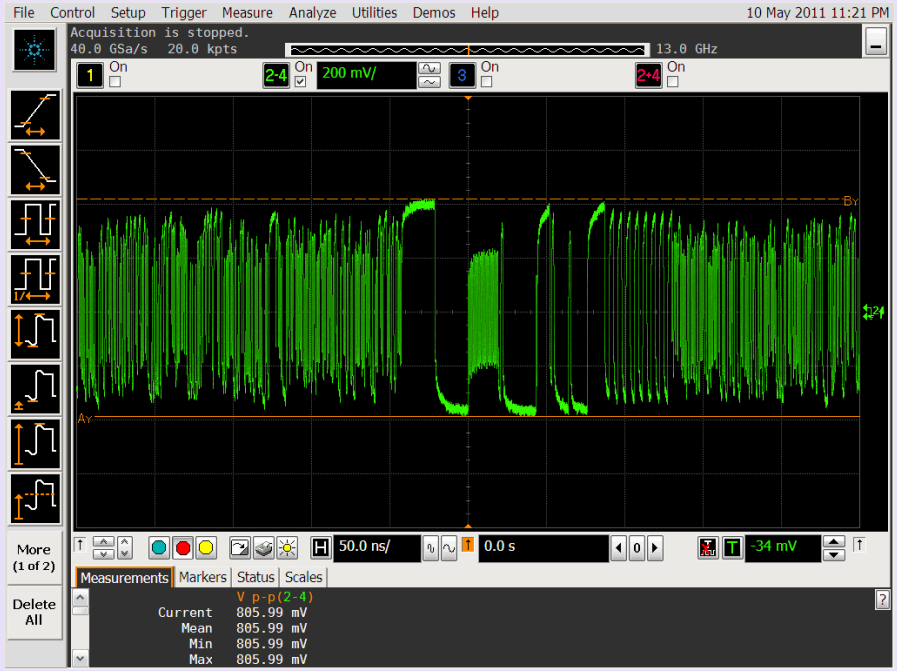
⇨ Combination of signal *measurements* and *SW-simulation* is required

Calibration Method of Stressed Eye for RX Test

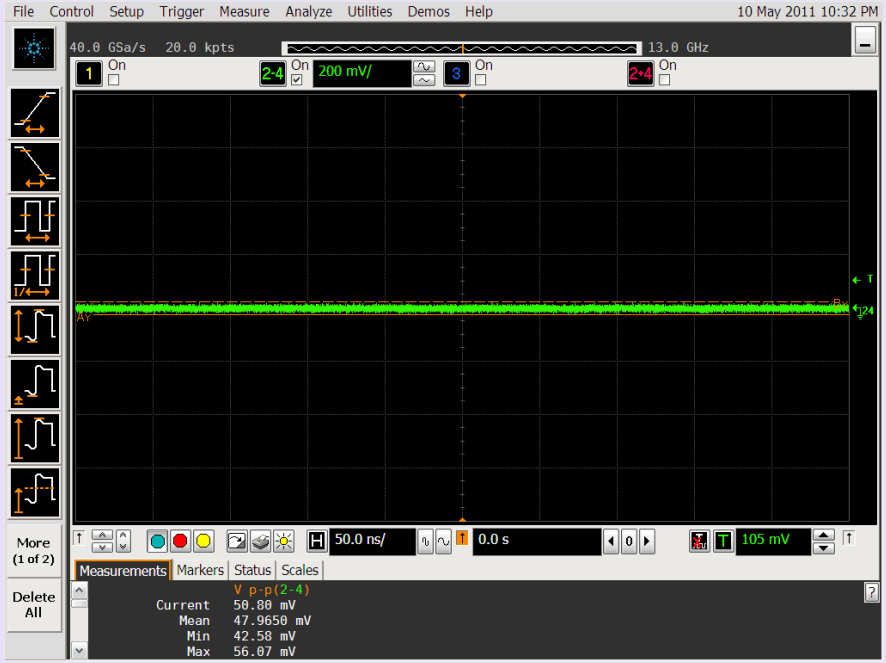


- Measure the actual RX test pattern with all signal impairments at TP2 and use SW to calculate the eye opening at TP2-P
  (applying package- and CDR- behavioral model and optimizing reference RX equalizers)
- Adjust the relevant impairments (such as DM-SI or RJ) on the test generator until the specified eye-height or eye-width is achieved
- Noise floor of RT-scope decreases eye-opening vertically
  and (through voltage-noise to jitter conversion) horizontally as well
  such that the resulting stress signal would be wider open than “measured”
  and the RX under test would not be stressed as much as intended

Screenshots of test pattern with impairments turned on



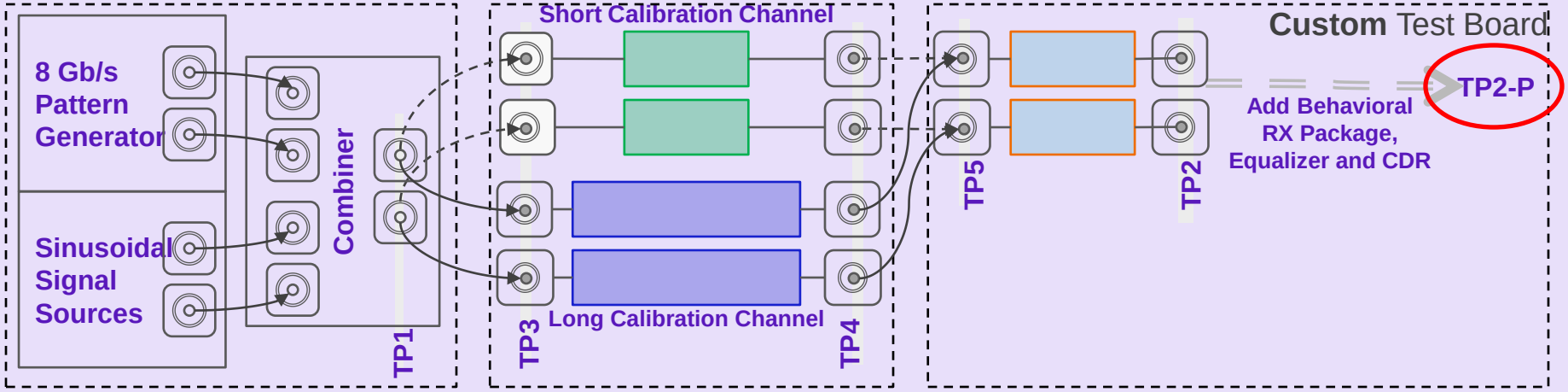
- Compliance pattern (800mV,pp) superimposed with DM-SI of $14mV_{pp}$ at 2.1GHz
- Scope setting 200mV/div (diff.) and a noise floor of approx. $4.7mV_{rms}$ (diff.)



- Same scope setting 200mV/div
- Pattern paused “visualizing“ DM-SI of $14mV_{pp}$ at 2.1GHz
- Reading of approx. 50mVpp !

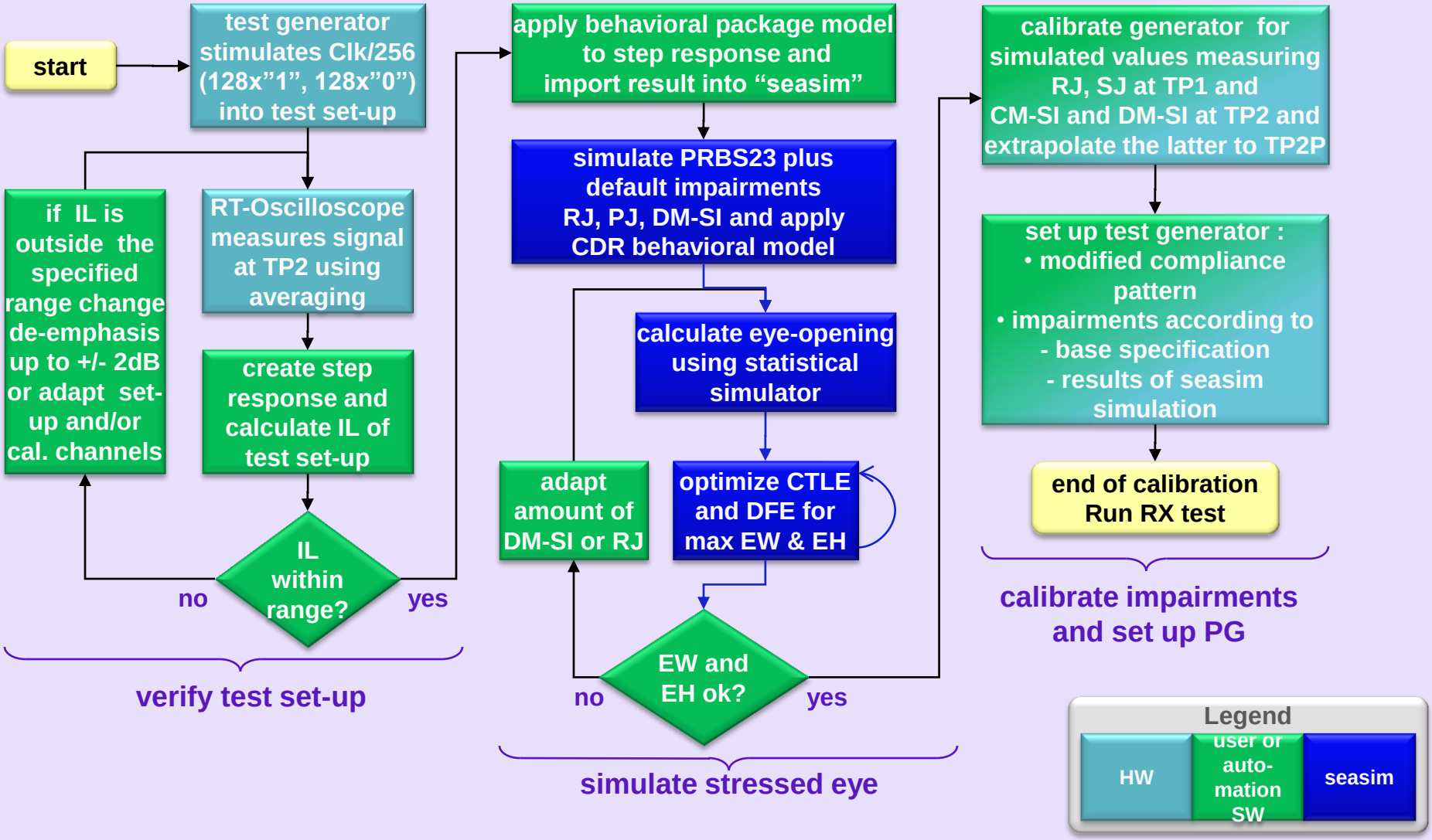
⇨ Accurate measurement of the stress signal at TP2 is impractical and error prone

Calibration Method of Stressed Eye for RX Test



- Divide the calibration of the RX stress signal into three separate steps:
  1. Characterize the test set-up at TP2 using a test signal (clock/256), which allows averaging for noise reduction of RT-scope, resulting in a measured “step-response”
  2. Use this step response as input for the statistical simulation SW that is also used for channel compliance verification and that calculates the eye opening for the final stress test signal (PRBS23) at a probability level of 10^{-12} after optimizing all equalizers and simulating impairments, iteratively finding the necessary amount of DM-SI or RJ that yields the specified eye-height (EH) or eye-width (EW)
  3. Calibrate those impairments, which require calibration, one at a time, at the best suited test-point with the best suited test signal
- Perform RX test with modified compliance pattern and all impairments turned on

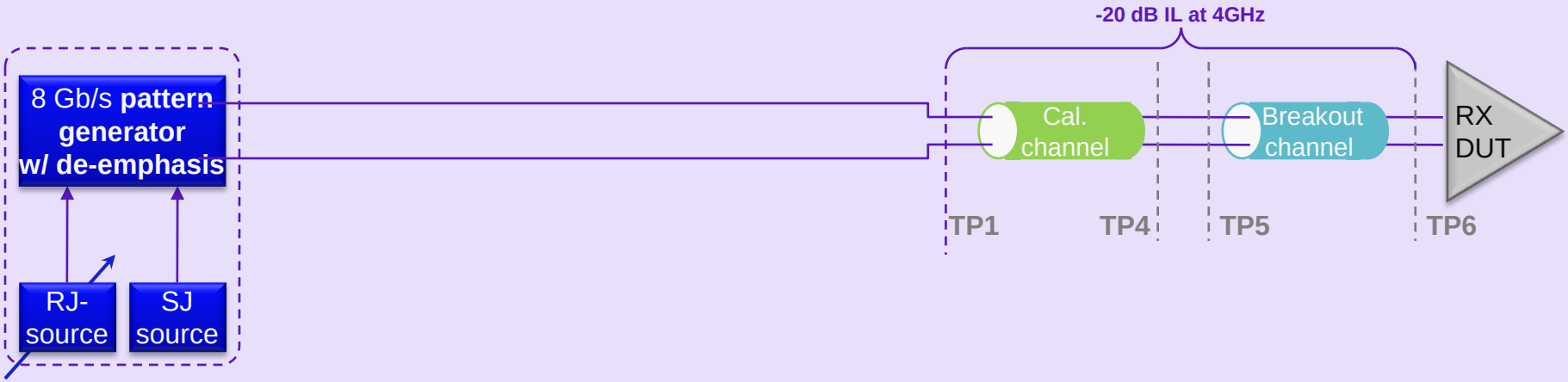
Calibration of Stressed Eye for RX Test
Flow chart w/ Statistical Eye Analysis Simulator (seasim)



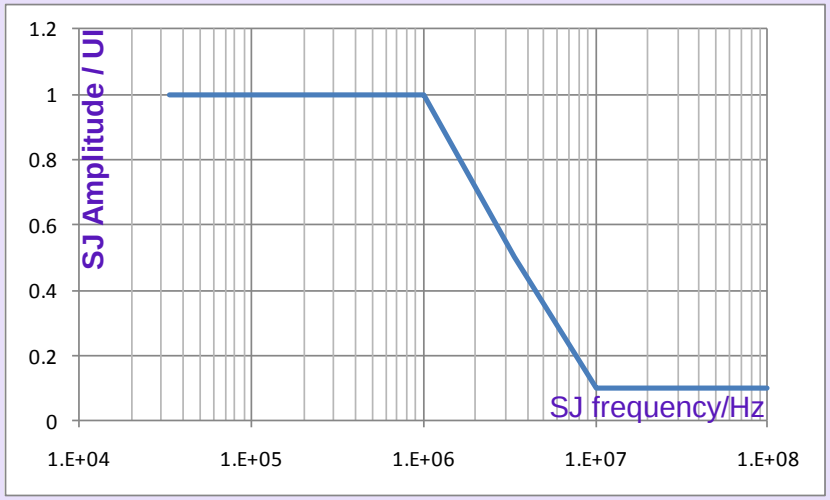
Agenda

- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

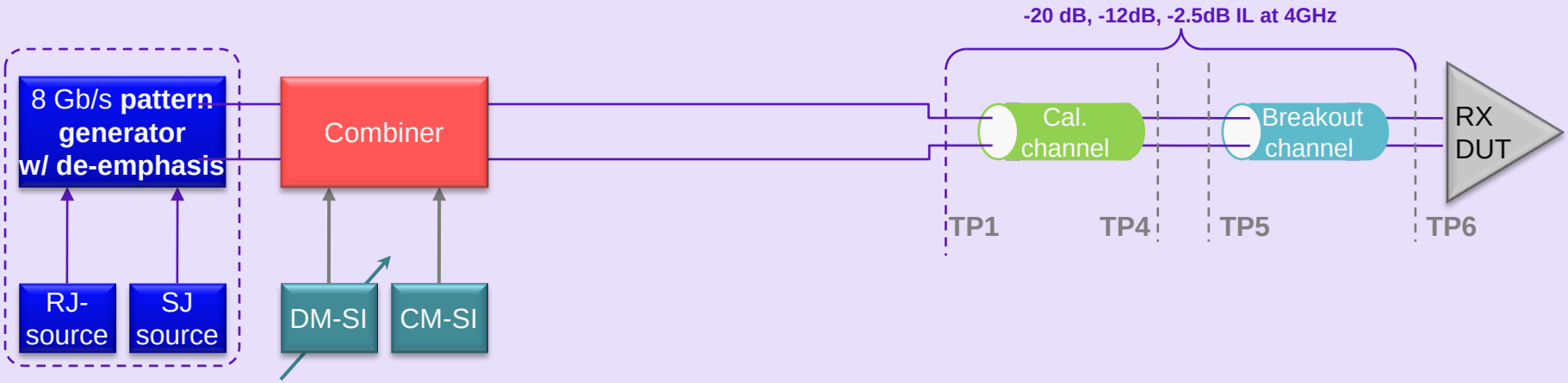
Two different RX Test Set-Ups (1 of 2) Stressed Jitter Eye



- Stressed *jitter* eye is testing RX for minimum horizontal eye opening (for long calibration channel plus break-out channel only)
- Horizontal eye closure adjusted varying RJ
- SJ varied according to specified curve
- This set up is straight forward and can be realized with suitable BERTs

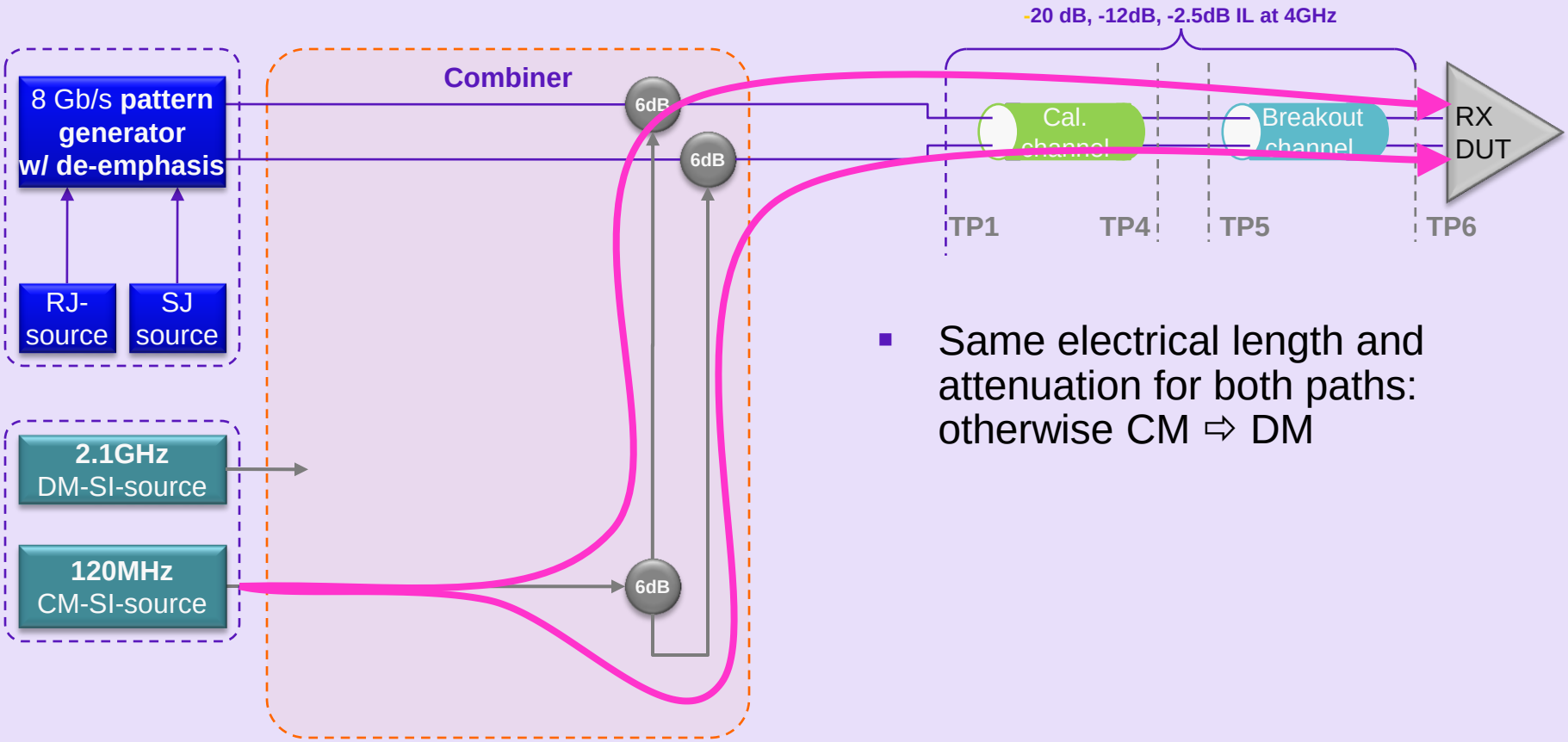


Two different RX Test Set-Ups (2 of 2) Stressed Voltage Eye



- Stressed *voltage* eye is testing RX for minimum vertical eye opening (three possible combinations of calibration- plus break-out- channels)
- Vertical eye closure is adjusted varying DM-SI
- **This test requires at least two additional voltage sources plus the non-trivial combiner circuit**

Realization for Voltage Interference Sources and Combiner



- Same electrical length and attenuation for both paths: otherwise CM ⇨ DM

- The most obvious realization for the CM-SI path
- DM-SI path not shown for simplification

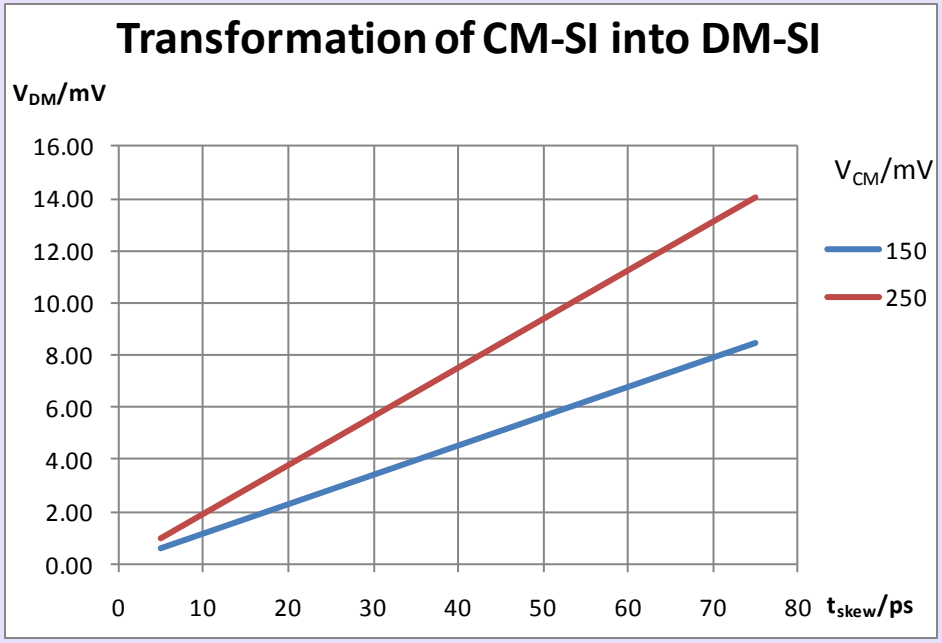
Transformation of CM- to DM-SI due to skew between "P" and "N"

$V_{DM}(t) = V_{CM,amp} \times \{\sin[\omega_{CM}t] - \sin[\omega_{CM}(t - t_{skew})]\}$

$\sin(x) - \sin(y) = 2 \times \cos((x+y)/2) \times \sin((x-y)/2)$

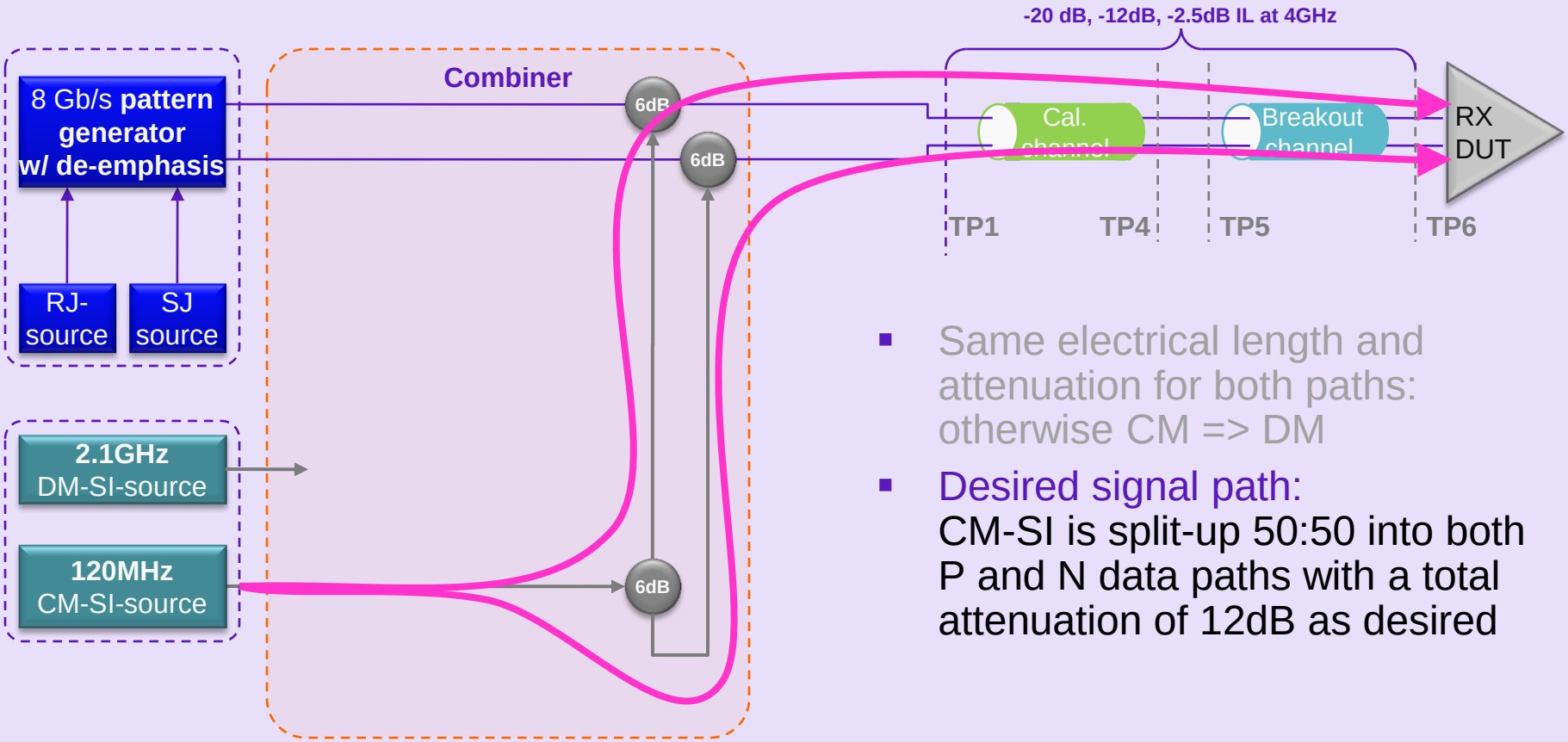
$V_{DM}(t) = 2 \times V_{CM,amp} \times \cos(\omega_{CM}(t - t_{skew}/2)) \times \sin(\omega_{CM}t_{skew}/2)$

$V_{DM,amp} = 2 \times V_{CM,amp} \times \sin(\pi \times f_{CM} \times t_{skew})$



In addition to DM-SI resulting from skew between the two sinewaves there is also DM-SI resulting from different amplitudes of the two sinewaves, which is directly proportional to amplitude and attenuation differences

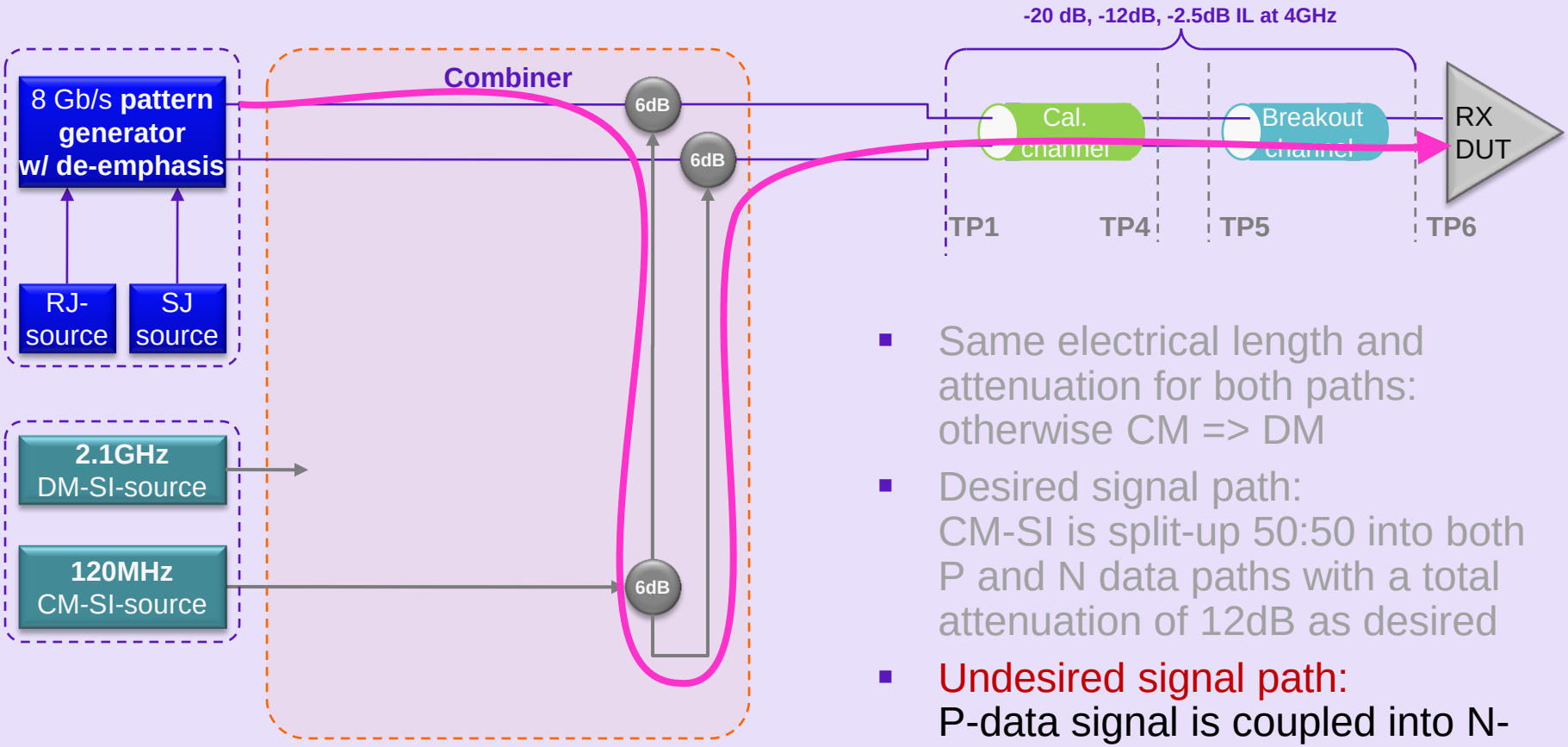
Realization for Voltage Interference Sources and Combiner



- Same electrical length and attenuation for both paths: otherwise CM => DM
- Desired signal path:
  CM-SI is split-up 50:50 into both P and N data paths with a total attenuation of 12dB as desired

- The most obvious realization for the CM-SI path
- DM-SI path not shown for simplification

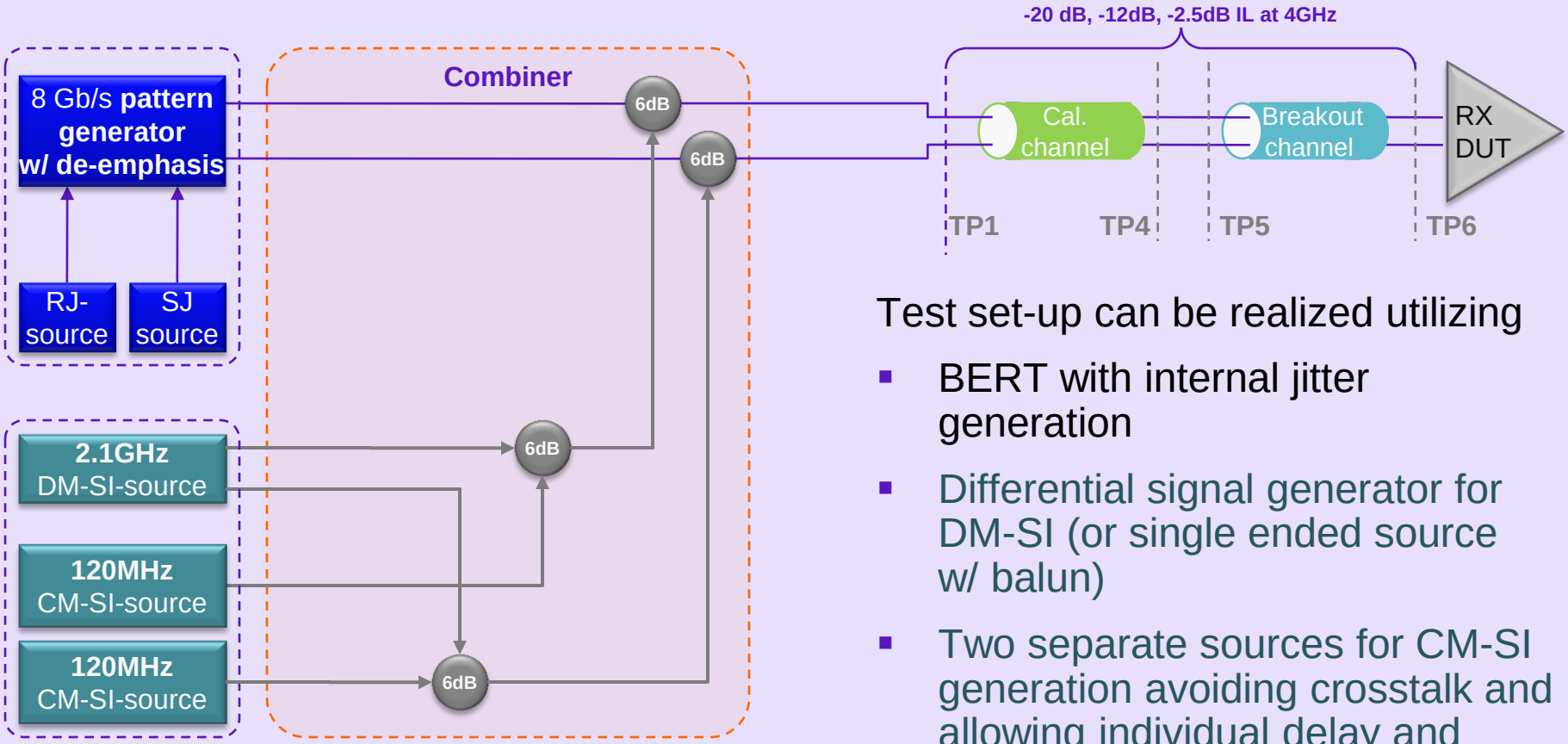
Realization for Voltage Interference Sources and Combiner



- The most obvious realization for the CM-SI path
- DM-SI path not shown for simplification

- Same electrical length and attenuation for both paths: otherwise CM => DM
- Desired signal path: CM-SI is split-up 50:50 into both P and N data paths with a total attenuation of 12dB as desired
- Undesired signal path: P-data signal is coupled into N-data signal path (and vice versa) with an attenuation of 12dB relative to the data signal generating undesired broadband (DC-coupled) crosstalk

Realization for Voltage Interference Sources and Combiner



- Final realization

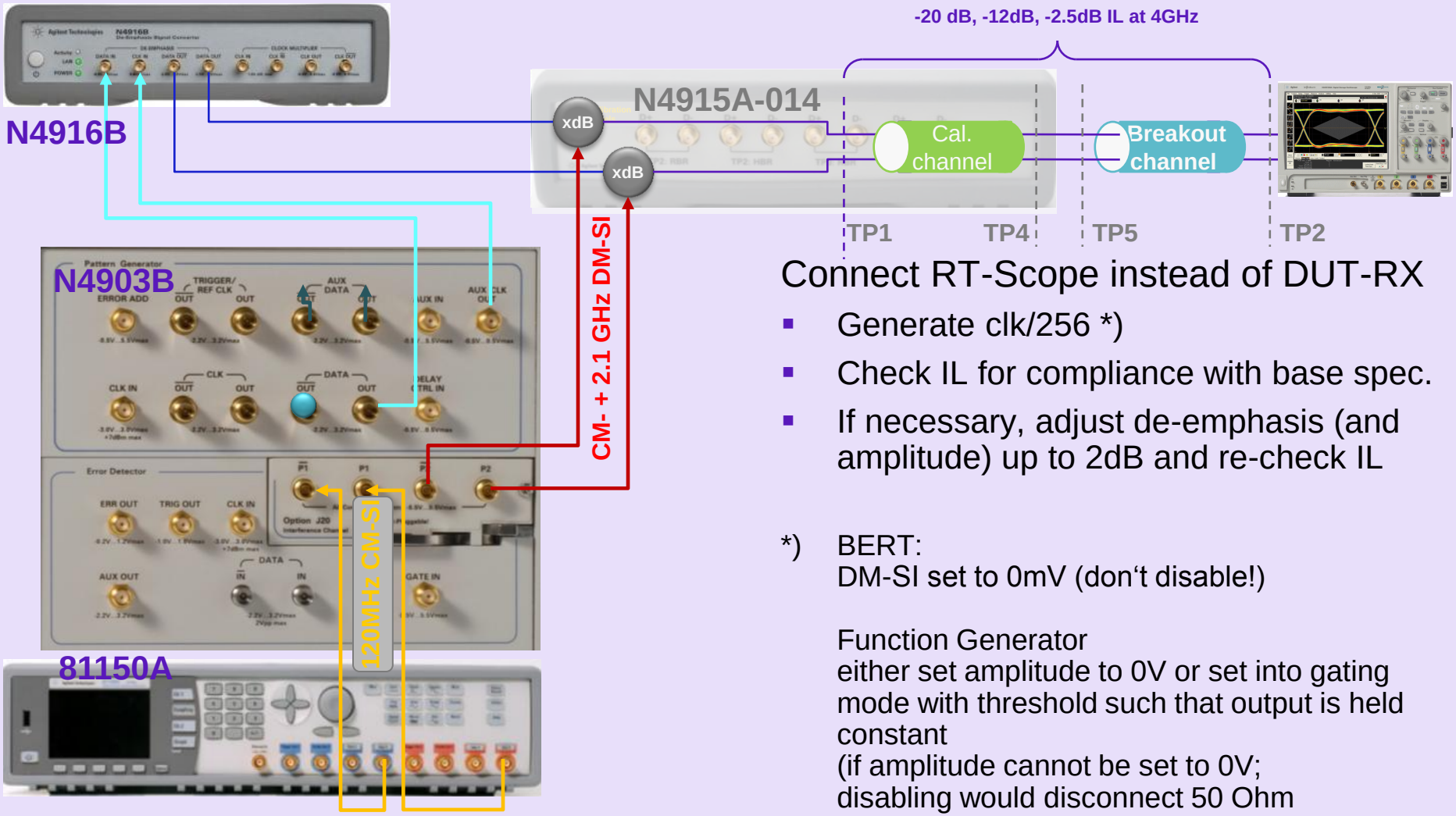
Test set-up can be realized utilizing

- BERT with internal jitter generation
- Differential signal generator for DM-SI (or single ended source w/ balun)
- Two separate sources for CM-SI generation avoiding crosstalk and allowing individual delay and amplitude adjust
- External “plumbing“ for signal addition

Agenda

- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

Calibration of Stressed Eye



Connect RT-Scope instead of DUT-RX

- Generate clk/256 *)
- Check IL for compliance with base spec.
- If necessary, adjust de-emphasis (and amplitude) up to 2dB and re-check IL

*) BERT:
DM-SI set to 0mV (don‘t disable!)

Function Generator
either set amplitude to 0V or set into gating mode with threshold such that output is held constant
(if amplitude cannot be set to 0V; disabling would disconnect 50 Ohm termination!)

Interpretation of Calibration Channel Specification

4.3.4.3.1. Calibration Channels

. . . The calibration channel's electrical characteristics are defined in terms of differential insertion loss masks as shown in Figure 4-66, with S_{21} measured between TP1 and TP2. Any HF loss caused by the generator and combiner and the connections between TP1-TP3 and TP4-TP5 that represent cabling are to be included in the S_{21} measurement.

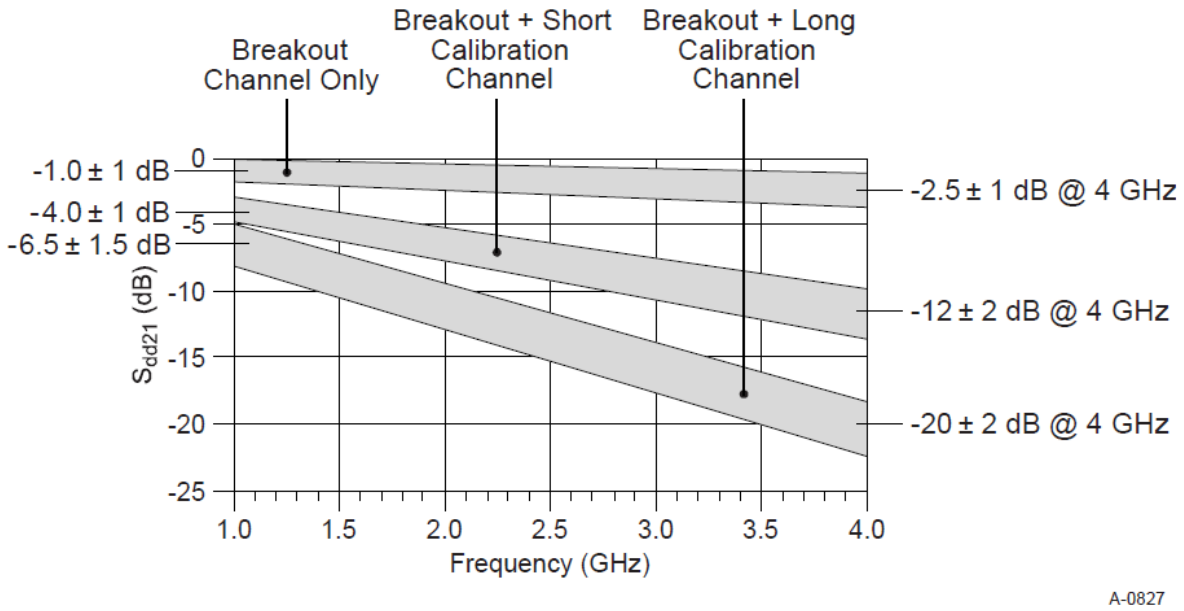
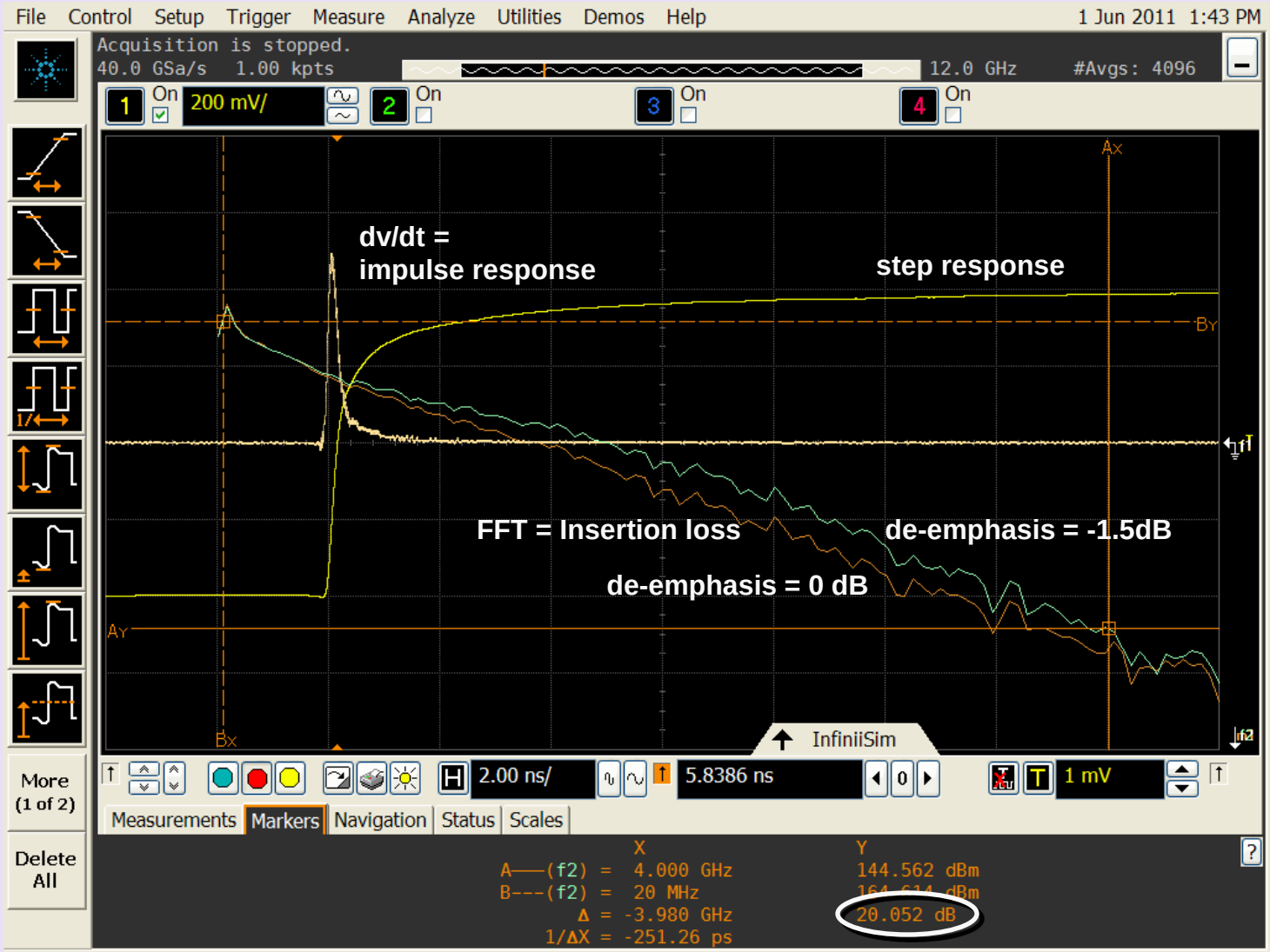


Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels

Long Cal. Channel with 0dB and -1.5dB De-emphasis

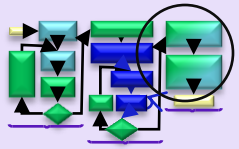


1. Check IL of test set-up: differentiating step response and doing FFT of the resulting impulse response
2. Measured IL too large (~21.5dB)!
3. Correct with appropriate de-emphasis of -1.5dB of post cursor and adjust amplitude for same end value of step response
4. Insertion loss of adjusted set-up ~ 20.0dB

Long Cal. Channel + Ref. Package

Apply the reference package model (IL @ 4GHz ~ 3.2dB) and import waveform in appropriate form into seasim!

Construction and Calibration of stress signal

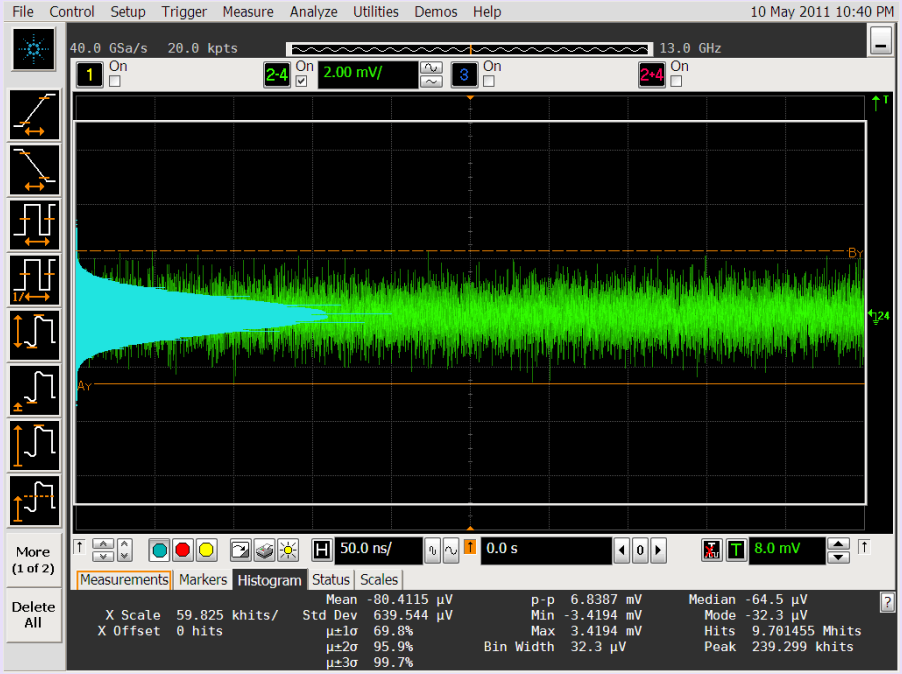


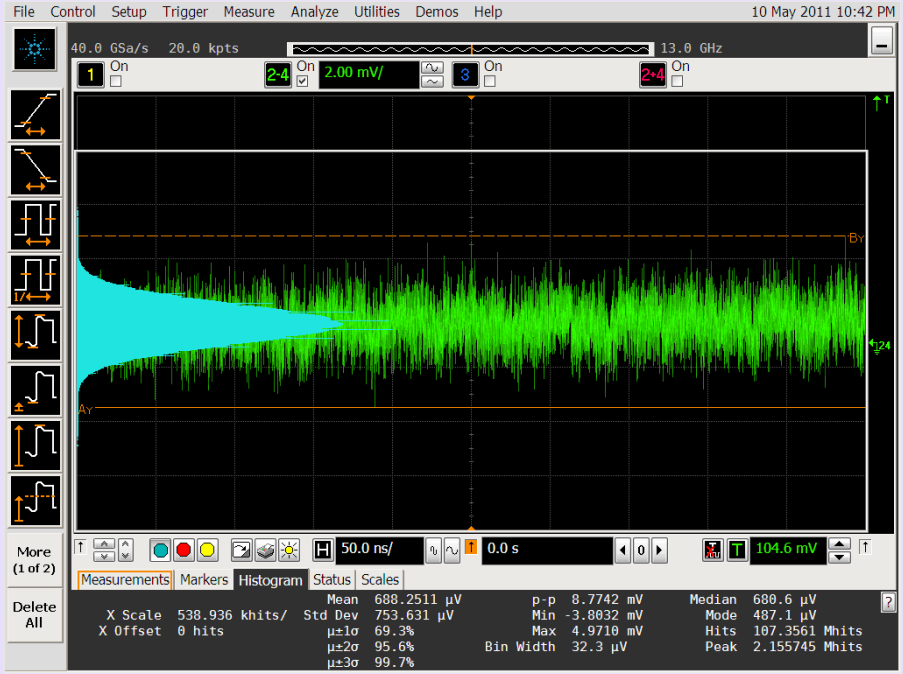
- Disconnect all signals from scope input (terminate with 50 Ohms)
  1. Measure* scope intrinsic noise $V_{n,intrinsic}$
- Turn on all sources, set generator to “pause“-pattern / set amp=0V (“disable“ outputs)
  2. Measure* Noise Voltage $V_{n,system}$ and determine noise of generators as $V_{n,gen} = \text{sqrt}\ (V_{n,intrinsic}^2 - V_{n,system}^2)$

* always apply ref. package model

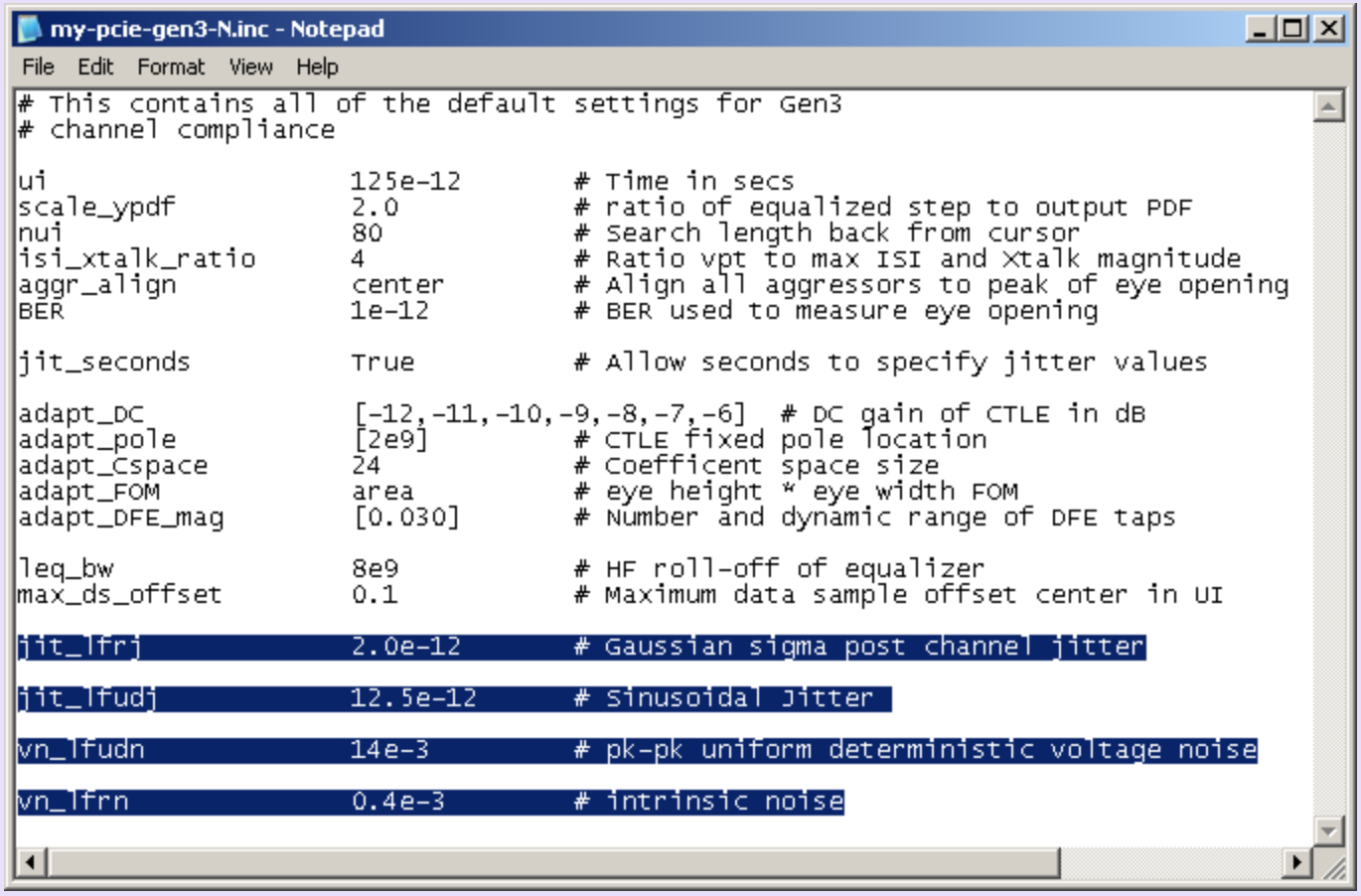
Differential Noise Voltage

- Scope Noise $V_{n,intrinsic} = 640\ \mu V_{rms}$
- System Noise = $V_n = 754\ \mu V_{rms}$
- $V_{n,gen} = \text{sqrt}\ (V_{n,intrinsic}^2 - V_{n,system}^2) = 399\ \mu V_{rms}$



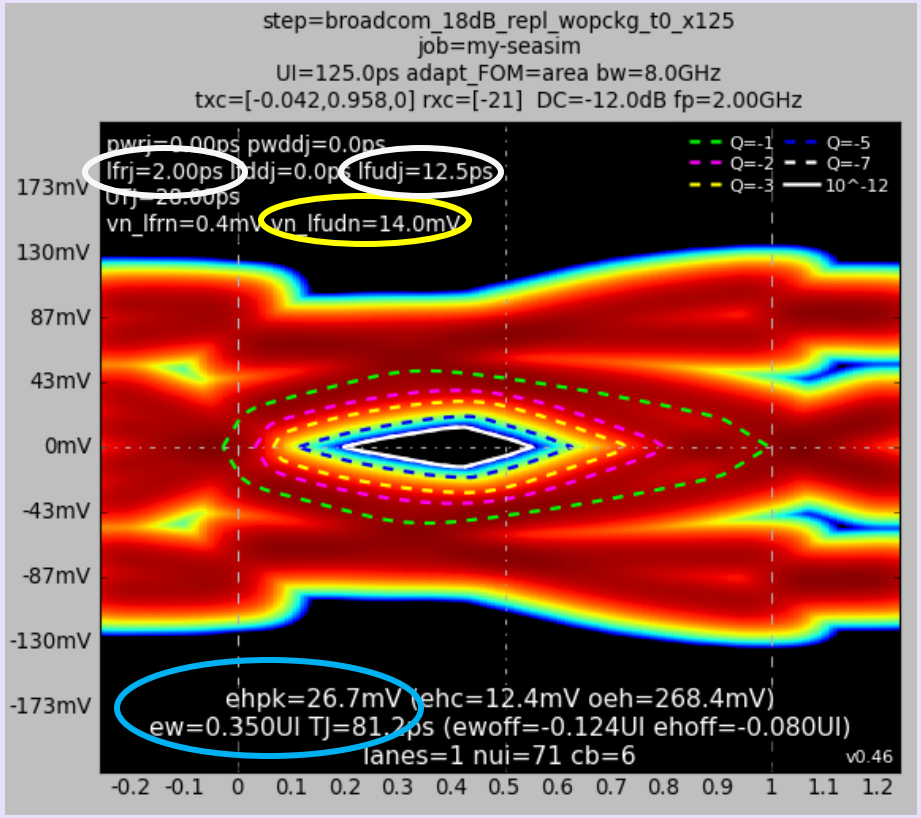


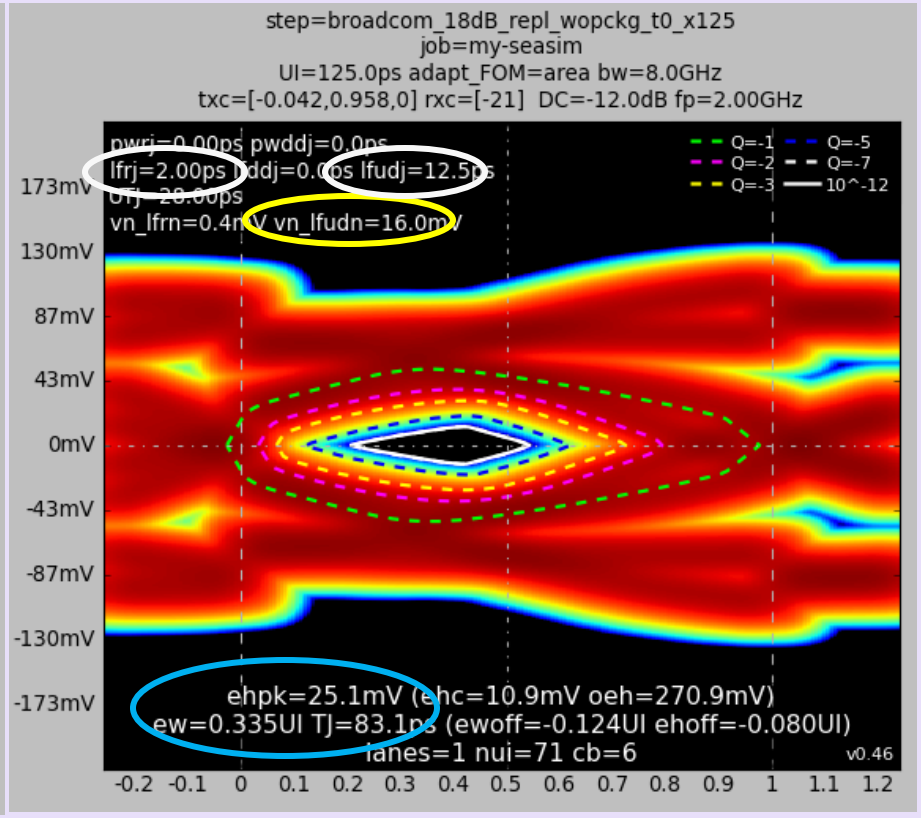
Seasim Parameters



RJ →
SJ →
DM-SI →
$V_{n,gen}$ →

Seasim calibration for stressed *voltage* test, long cal channel

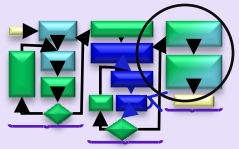




starting value for DM-SI = 14mV
resulting in ~27mV of eye height (EH)

“SW-adjusted“ value for DM-SI = 16mV
resulting in ~25mV of EH w/ (0.3UI<EW<0.35UI)

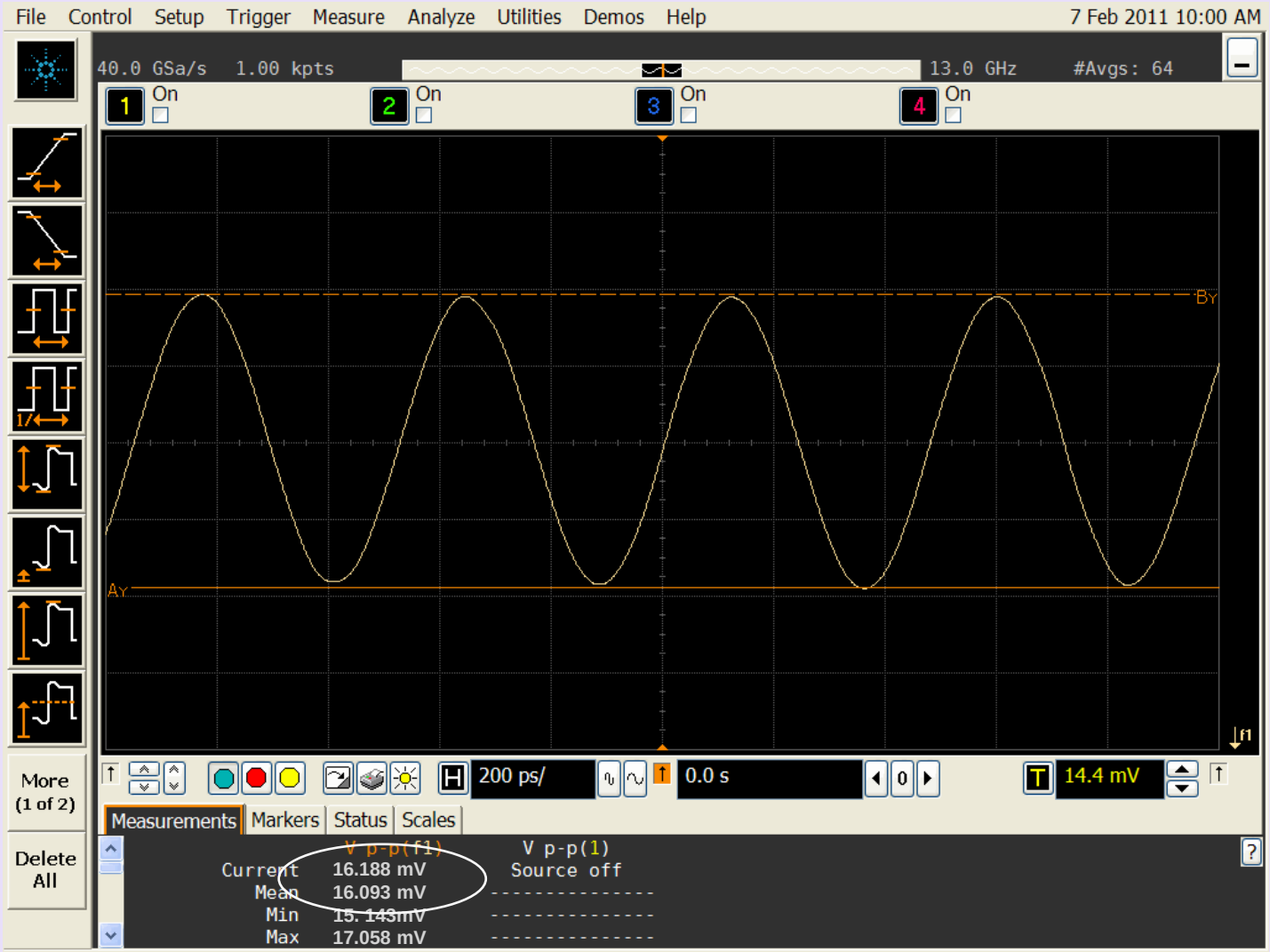
Construction and Calibration of stress signal



- Disconnect all signals from scope input (terminate with 50 Ohms)
  1. Measure* scope intrinsic noise $V_{n,intrinsic,rms}$
- Turn on all sources, set generator to “pause“-pattern / set amp=0V (“disable“ outputs)
  2. Measure* Noise Voltage $V_{n,system}$ and determine noise of generators as
     $V_{n,gen} = sqrt (V_{n,intrinsic}^2 - V_{n,system}^2)$
  3. Adjust* DM-SI voltage amplitude to value resulting from Seasim

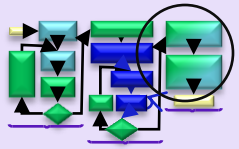
* always apply ref. package model (package loss at 2.1 GHz approximately 1.7dB)

Calibration of 2.1G DM-SI



As $V_{n,gen}$ (noise from generator) is taken care of by vn_lfrn in seasim, averaging can be used for calibration of DM-SI

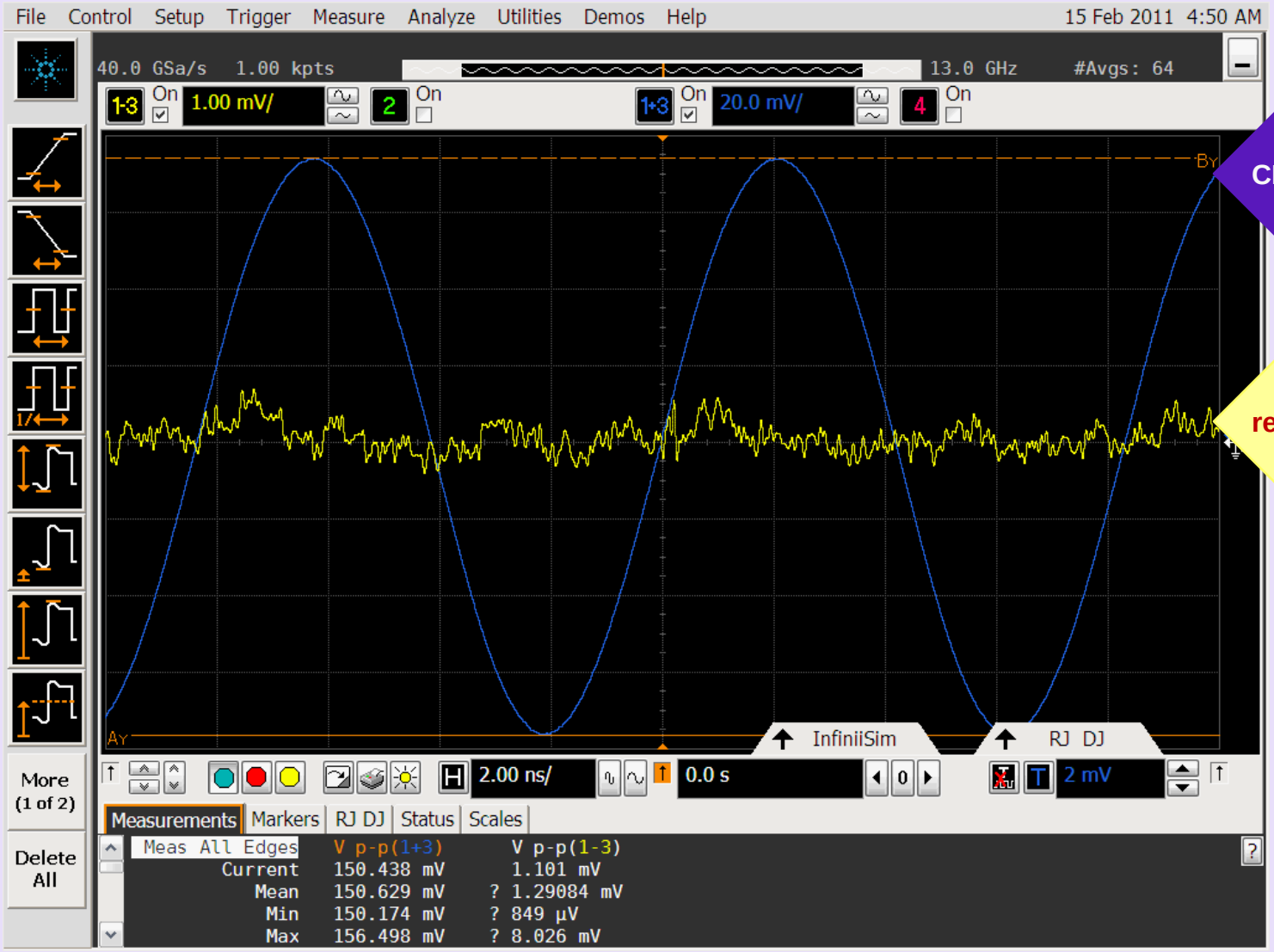
Construction and Calibration of stress signal



- Disconnect all signals from scope input (terminate with 50 Ohms)
  1. Measure* scope intrinsic noise $V_{n,intrinsic,rms}$
- Turn on all sources, set generator to “pause“-pattern / set amp=0V (“disable“ outputs)
  2. Measure Noise Voltage $V_{n,system}$ and determine noise of generators as $V_{n,gen} = sqrt (V_{n,intrinsic}^2 - V_{n,system}^2)$
  3. Adjust DM-SI voltage amplitude to value resulting from Seasim applying ref. package model
     (package loss at 2.1 GHz approximately 1.7dB)
  4. Adjust CM-SI amplitude to specified value (150 or 250mV)
     (also applying ref package model)
     adjust delay (and amplitudes) of CM-SI generator for minimum residual differential amplitude

* always apply ref. package model

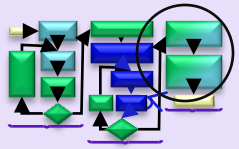
CM-SI calibration of residual DM



CM-SI, 120MHz 150mV

remaining DM –“noise“

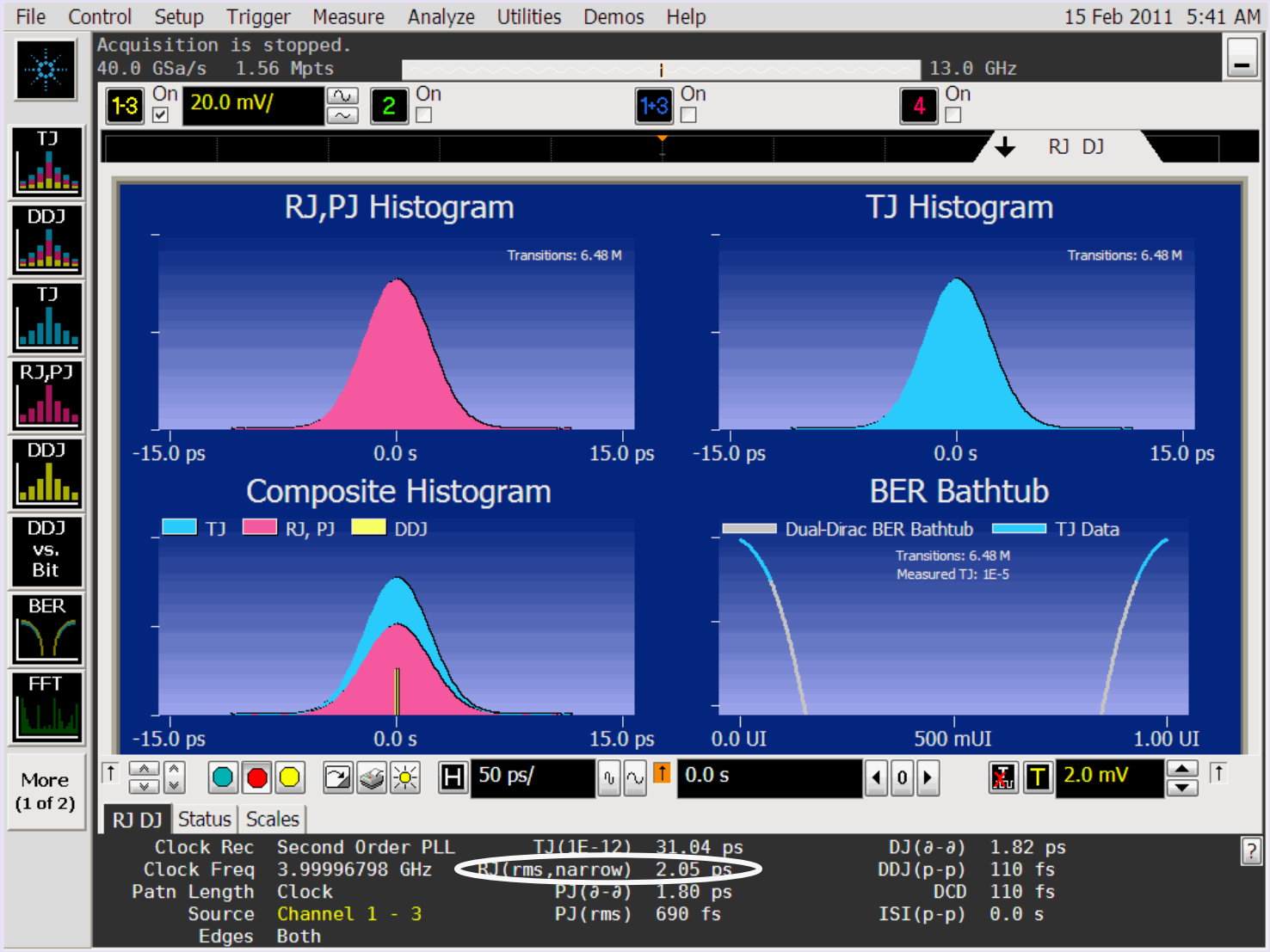
Construction and Calibration of stress signal



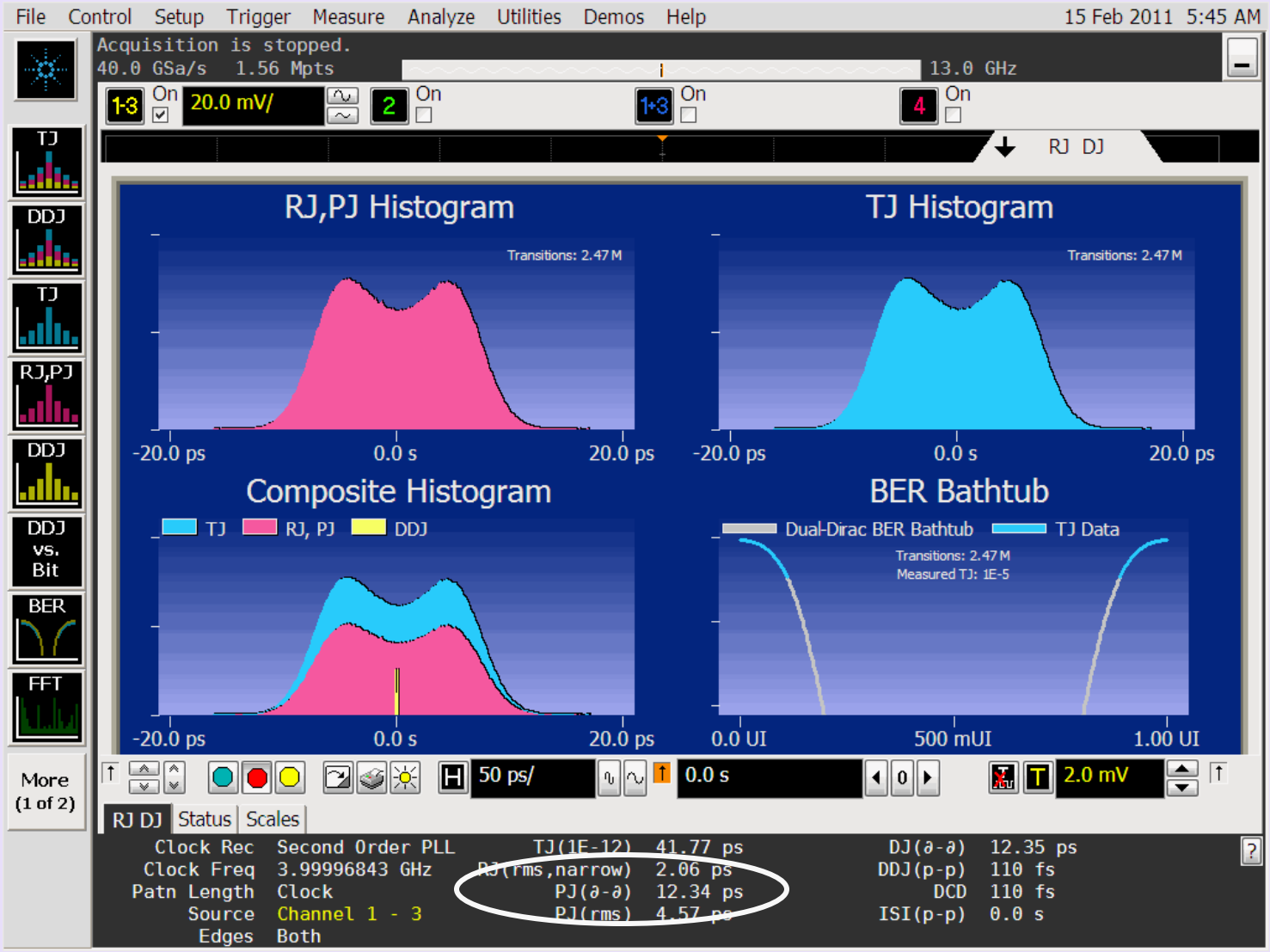
- Disconnect all signals from scope input (terminate with 50 Ohms)
  1. Measure* scope intrinsic noise $V_{n,intrinsic,rms}$
- Turn on all sources, set generator to “pause“-pattern / set amp=0V (“disable“ outputs)
  2. Measure* Noise Voltage $V_{n,system}$ and determine noise of generators as $V_{n,gen} = sqrt (V_{n,intrinsic}^2 - V_{n,system}^2)$
  3. Adjust* DM-SI voltage amplitude to value resulting from Seasim applying ref. package model
     (package loss at 2.1 GHz approximately 1.7dB)
  4. Adjust* CM-SI amplitude to specified value (150 or 250mV)
     (also applying ref package model)
     adjust delay (and amplitudes) of CM-SI generator for minimum residual differential amplitude
  - ✓ Set generator to clock/2 pattern
  5. Turn on RJ and SJ each at a time and sequentially adjust* them to specified values measuring either at TP1 or TP2

* always apply ref. package model

Calibration of RJ

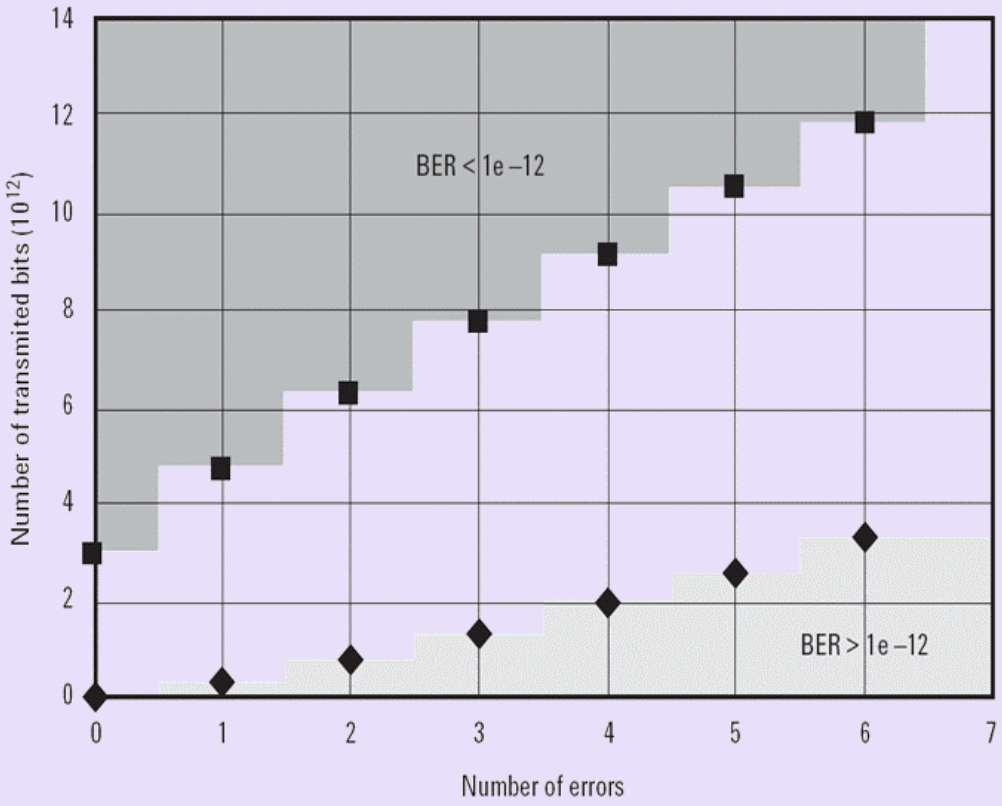


Calibration of RJ and SJ



Calibration accomplished - ready to perform the RX test

- Disconnect cables fromTP5 (input replica channel) and connect to TP6 (input breakout channel)
- Set DUT-RX into loopback
- Turn on all impairments as calibrated and make BERT-PG generate the test pattern (modified compliance pattern)
- Verify number of errors for sufficient time period such that BER<10^{-12} w/ 95% of CL
  e.g.:
  0 errors in 6¼ minutes
  1 error in 10¼ minutes
  2 errors in ...



Agenda

- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

Summary

- PCIe 3.0 Phy Layer system design with its 8GT/s was relatively demanding, its realization in a computer system is not trivial
- Interoperability depends on proper RX functionality and can only be guaranteed by thorough RX testing
- Test set-up must be designed with great care
- Calibration of stress test signal requires deep insight into base specification and measurement techniques
- Performing “step-by-step calibration“ manually is cumbersome and error prone – automation desirable

Agenda

- From PCIe 2.x to PCIe 3.0
- Test Set-up and Calibration Methodology according to Base Specification
- Practical set-up
- Step-by-step Calibration Procedure
- Summary
- Q&A

Thank you for attending the
PCI-SIG Developers Conference 2011.

For more information please go to
www.pcisig.com